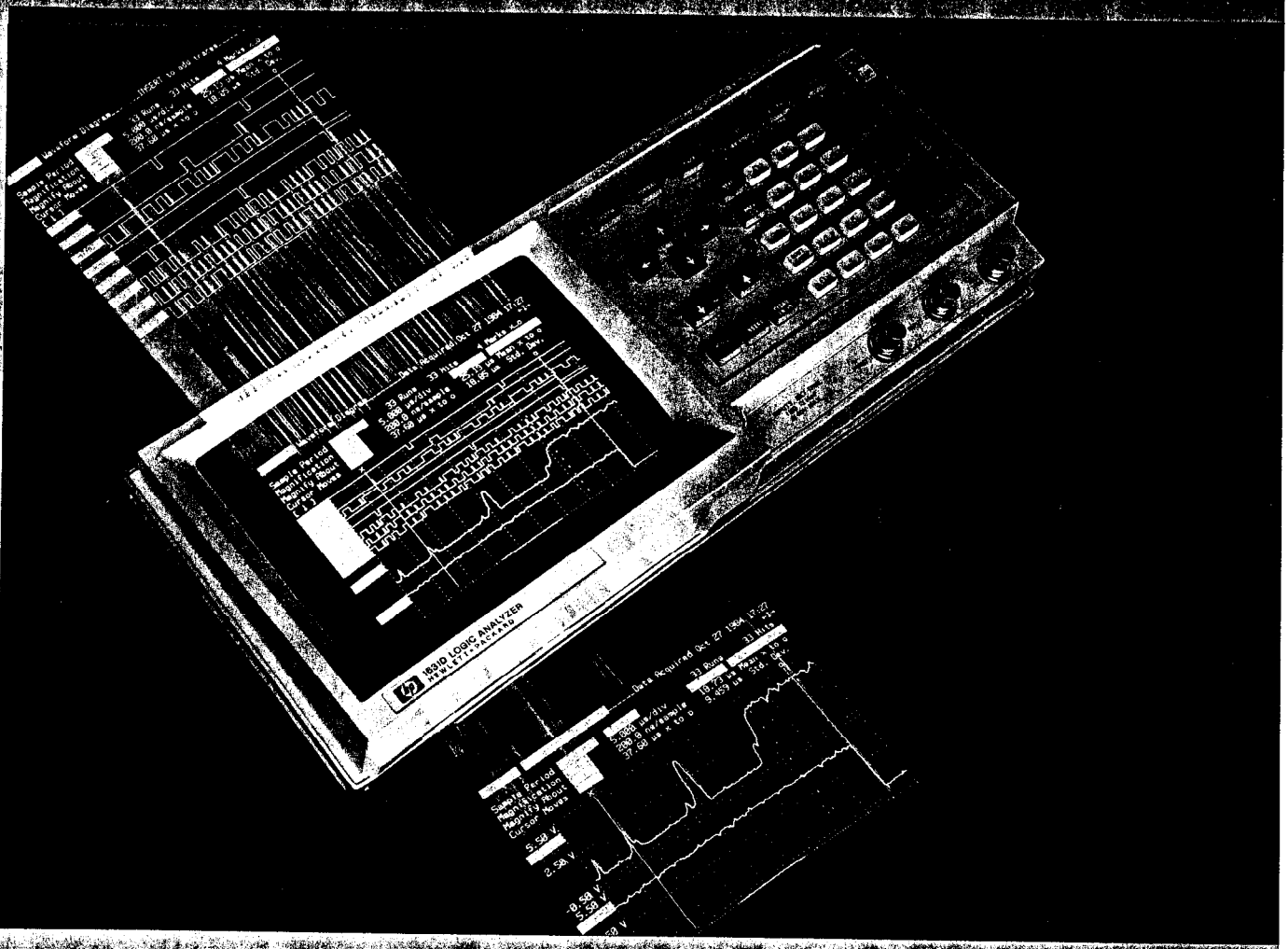
Measurement/Reference Guide

For The HP 1631A/D Logic Analyzer

the one with the scope

HEWLETT PACKARD



Contents

Measurement Feature Matrix

	Measurement Number									
Feature	1	2	3	4	5	6	7	8	9	10
Analog Triggering	A	A	B							
Analog Markers (Voltage, Time)			A	B						
Analog Post-processing				A						
Glitch Capture								A	B	
Timing Post-processing (Cursors)						A	A			
Timing Triggering					A	B	B			
Timing Arms Analog (Simultaneous **Capture**)									A	
State Triggering										A
Mixed Display (Timing Analog)									B	
Fast Analog Sample Rate		B								

A primary focus
B secondary focus

Abstract Of Measurements

Measurement 1: capturing and displaying the 4 MHz signals from the HP 5036A crystal with the digitizing oscilloscope. Includes an example of how to set trigger conditions for the scope.

Measurement 2: looking at transients on the +5V power supply line of the HP 5036A. Shows how a digitizing oscilloscope can trigger on events that it may not be able to display because of a long specified sample period.

Measurement 3: uses the x and o markers in the oscilloscope to measure a voltage-dependent time interval between the +5V power supply and the L = RESET IN line to the 8085.

Measurement 4: an introduction to using the analog post-processing capabilities to make certain the voltage-dependent time interval of measurement 3 does not violate manufacturers specifications.

Measurement 5: setting FORMAT and TRACE specifications and capturing six signals on the DRAM board with the timing analyzer. Includes a brief familiarization exercise on the timing analyzer.

Measurement 6: use of timing post-processing capabilities to measure how long the microprocessor is idle during a forced refresh. Starts with ballpark calculations from the manufacturers specification sheet then determines actual maximum time by using the post-processing time interval measurement features. Uses the results to determine how asymmetrical the DRAM refresh clock can be to improve efficiency.

Measurement 7: continuation of measurement 6 to determine average idle time of the microprocessor during simulated normal operation. While measurement 6 looked at only forced refreshes, this measurement includes forced and hidden refreshes. Looks at the difference in idle time between symmetrical and asymmetrical DRAM refresh clocks.

Measurement 8: an introduction to glitch capture with the timing analyzer. Shows how to set TRACE specifications for glitch mode and captures a recurring glitch on the DRAM board.

Measurement 9: continuation of measurement 8 using time-correlated analog and timing to determine cause of the glitch. Shows mixed display mode where both analog and timing channels are on the same screen.

Measurement 10: an introduction to the state analyzer. Captures a simple state listing and shows how to inverse assemble the listing.

Equipment List

Following is a list of the equipment needed to make the measurements discussed. Each measurement lists the appropriate connections from the logic analyzer to the HP 5036A Microprocessor Lab.

- HP 1631D logic analyzer
- HP 10017A 10:1 divider probes (two each, supplied with the HP 1631D)
- HP 5036A microprocessor lab with DRAM board (DRAM board available from the HP Colorado Springs Division)
- HP 9121S/D or 9122S/D discdrive
- HP 10269B probe interface
- HP 10304B 8085 interface module with inverse assembler
- Disc 20-pin IC clips (2 each)

Introduction

The purpose of this Measurement Reference Guide is to acquaint you with some of the features and capabilities of the 1631. It is not intended to be a complete guide to every feature, but rather to give insight into the types of measurements the 1631 can make. As much as possible, each measurement is related to the types of problems encountered by a design engineer. It does assume some level of experience in using analog oscilloscopes, but does not assume any level of expertise with a logic analyzer. With that in mind, the guide starts out in the realm of the oscilloscope and progresses into the world of logic analysis. It also addresses areas where the mating of the two yields significant advantages. Many of the measurements discussed have been previously impossible, or at best very difficult.

Should you need it, Appendix B is a brief tutorial on the format and trace specification menus that relate to each portion of of the analyzer. The tutorial describes each field in the menu for that particular portion. As each section of the guide progresses, additional menus are shown to help you set up the measurement. More information on the menus is available in the HP 1631A/D operating and programming manual (HP part # 01631-90901).

The looseleaf format of this guide was chosen to allow for expansion. It is our goal to fill the measurement/feature matrix that follows the table of contents. Although the initial printing does not do this, it will be finished after introduction of the 163 1. Notification of additional measurements for the guide will be made in the HP Instrument News letter. While many of the measurements are continuations of previous ones, the matrix should provide a reference for determining which measurements in the guide exercise which features of the 163 1.

Using The Digitizing Oscilloscope Within The HP 1631A/D

Introduction To Digitizing Oscilloscopes

Although most of us are familiar with the traditional analog oscilloscope, and perhaps even an analog storage oscilloscope, a digitizing storage oscilloscope offers a number of advantages. Some of these are demonstrated in the first section of this guide, but are mentioned here for sake of introduction.

One problem with an analog storage oscilloscope is its tendency to bloom or fade. Even the best of storage scopes loose their image with time, due to these factors. A digitizing oscilloscope does not suffer from this because it does not store the image on a mesh in the CRT, but rather in semiconductor memory. Because the image is stored in memory, it can be retained on-screen indefinitely without degradation. In addition, the image can be dumped from memory to a printer or mass storage device for later recall. Since the information in memory is a digital representation of the actual waveform, it can be dumped to a computer for post-processing if desired. This can be important in production environments where a waveform is tested against a standard.

When a signal has a low duty-cycle or rep-rate that requires a long sweep speed for viewing, flicker becomes a very real problem, both in terms of annoyance and representation of the signal. Again, a digitizing oscilloscope provides a stable display of the waveform without flicker. It can do this because the waveform is kept on-screen until the next complete update is ready for display.

Often, it is helpful to view part of the waveform that occurred before the trigger point. For instance, suppose you need to look at the rising and falling edges of a sawtooth that is several milliseconds long. We suspect that the latter portion of the rising ramp is non-linear due to non-resistive loading. We can't trigger on the rising portion of the ramp and display it with an analog oscilloscope, due to its long period, so it would be very handy to trigger on the falling edge and look backward in time. The digitizing oscilloscope within the HP 1631A/D allows you to trigger on an edge and look backward in time to pre-trigger events. This capability is called negative time capture and is a fundamental feature in HP's digitizing oscilloscopes.

Digitizing oscilloscopes, although superior to analog oscilloscopes in many cases, make some compromises of which you should be aware. These are fundamentals in sampling theory and create inherent errors. On fast transitions, the digitizer can sample only a few points on the edge, and the hardware (or software, in the case of the HP 1631A/D) interpolator "fills in" the points in between. The digitizer must make some assumptions as to the shape, and can be optimized for either interpolator speed or accuracy of waveshape. If rise time is all-important, the interpolator can be optimized by arbitrarily changing the shape of the edge by adding preshoot and overshoot. If the accuracy of waveshape is of primary concern, rise time capture will be slower. The HP 1631A/D reaches a compromise between the two. The fidelity of the waveshape is maintained while providing a minimum rise time display of 7 nanoseconds. This means that if you could generate a zero nanosecond rise time edge, the HP 1631A/D would display it as a 7 ns rise time edge. Obviously, as the rise time becomes longer, this inherent inaccuracy becomes less of a factor.

Using The Digitizing Oscilloscope Within The HP 1631A/D (continued)

Measurement 1:
Getting Started With The Digitizing Oscilloscope Within The HP 1631A/D.

Problem: using the HP 1631A/D as a real-time digital oscilloscope.

Description: look at the system clock in a continuous mode, with and without trigger qualification. When the HP 1631A/D is powered up, it is configured for use as a real-time scope. All that you need to do is connect the probes to the analyzer and signals and press the RUN key.

Setup: connect two HP 10017A probes to the channel 1 and channel 2 BNCs on the front panel beneath the keyboard. Connect channel 1 to pin 1 of the 8085 microprocessor in the HP 5036A microprocessor lab and channel 2 to pin 2 of the processor. Power up the HP 1631A/D and press the RUN key. You should have a 4 MHz signal on both channels 180 degrees out of phase with one another.

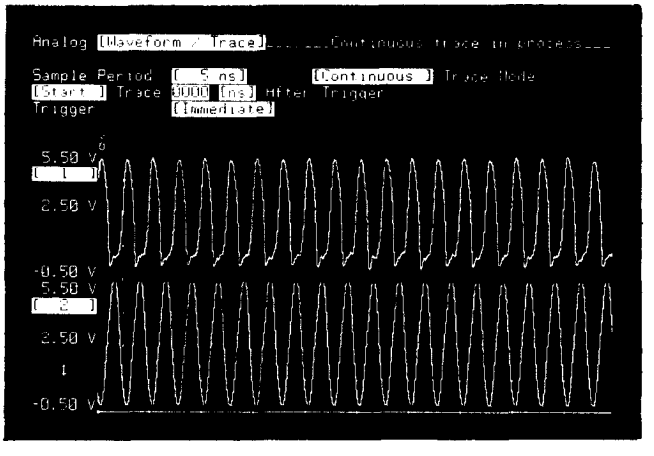


Figure 1

Notice that the message across the top of the screen tells you that you are in the analog portion of the analyzer and that you are using the [Waveform/Trace] display. This is the real-time oscilloscope display. Also notice that the analyzer is in the continuous mode.

Let's set a trigger condition for the oscilloscope. Using the CURSOR keys, move the cursor down to the field labeled [Immediate].* This is the trigger condition. [Immediate] means that the analyzer starts to store data as soon as the RUN key is pressed and that it has no qualification. Press the NEXT[ ] key. The trigger condition is now set for channel 1 and a rising edge with a trigger threshold of O.OOV. Move the cursor to the [Rising] field and press the NEXT[ ] key. The trigger edge is now [Falling]. Use the cursor keys to move to the trigger level field and enter a new threshold of 1.4 V from the HP 1631A/D's keyboard. The oscilloscope is now triggering on a falling edge of channel 1 at a threshold of 1.4 V. The trigger channel can be changed to channel 2 or to the external trigger channel.

One last condition of importance in this menu is the sample period. It can be changed from 5 ns to 500 ms in a 1-2-5 sequence.

Conclusion: congratulations! You have just made your first measurement with the HP 1631A/D. Although not too complicated, it demonstrates how easy it is to use the analog portion of the HP 1631A/D **as** a real-time digital oscilloscope. The following measurements and sections, we will investigate further the power of the 1631.

**There will be same delay between when you press the cursor key and when the cursor moves when the analyzer is running. This is normal, as the HP 1631A/D acts on keyboard presses only between acquisitions.*

Measurement 2:
Using The Digitizing Oscilloscope With A Trigger Condition.

Problem: trigger on and display power supply noise on the microprocessor +5 V supply line and the RESET line.

Description: the microprocessor has a RESET line that is used to initialize it on power-up. When the RESET line reaches threshold (2.4V), the processor starts normal operation. However, the line cannot just be connected to the 5 V power supply, because the microprocessor needs 10 ms between when the supply line reaches 4.75 V and when the RESET line crosses through the threshold. This allows time for an internal oscillator to stabilize. To make certain that the RESET line waits for at least 10 ms to cross threshold, an RC network is installed to integrate the power-on pulse.

When the system is powered up, several voltage excursions appear on the line. With an analog storage oscilloscope, these would be difficult to see and still keep the sweep speed low enough to see the slow RESET transition. We will look at these transitions with the 1631 to illustrate a basic advantage of a digitizing oscilloscope—the ability to capture and display low rep-rate signals stably.

Setup: power up the HP 1631A/D. On-screen is the System Configuration menu which shows the current configuration of the analyzer. At power up, the HP 1631A/D is configured for use with only two analog channels. This is the configuration we will use for the next three measurements.

Connect two HP 10017A probes to the channel 1 and channel 2 BNCs on the front panel beneath the keyboard. Connect channel 1 to pin 40 of the 8085 in the HP 5036A microprocessor lab. This is the +5 V supply line. Connect channel 2 to pin 36 of the 8085, which is the L = RESET IN line.

Press the FORMAT key, which is one of six along the top of the HP 1631A/D keyboard. This brings up the format configuration menu to allow you to set the format for the measurement. Change it to match figure 2.

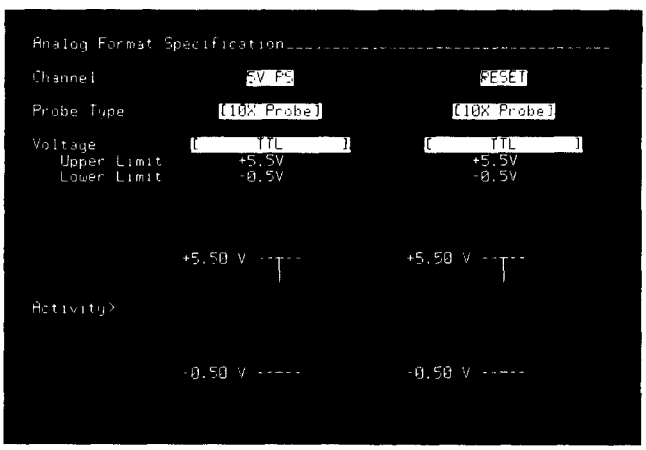


Figure 2

Press the TRACE key, which is one of six along the top of the HP 1631A/D keyboard. This brings up the trace configuration menu to allow you to set the trace conditions for the measurement. Change it to match figure 3.

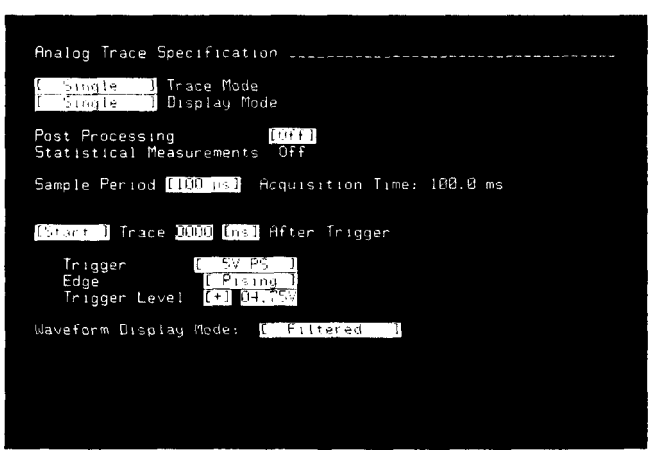


Figure 3

Power the 5063A off. Press the RUN key on the HP 1631 and power up the HP 5036A. Be sure to wait 4 or 5 seconds between when power to the HP 5036A is turned off and then turned on again to allow the power supply filter capacitors to discharge. A display similar to figure 4 should be on-screen.

Note: the +5 V power supply in some HP 5036As may not reach 4.75 volts. If you have one, change the trigger voltage for channel 1 of the 1631 to 4.5 volts. This is not the voltage specified by the manufacturer, but will still Serve to illustrate the point.

Using The Digitizing Oscilloscope Within The HP 1631A/D (continued)

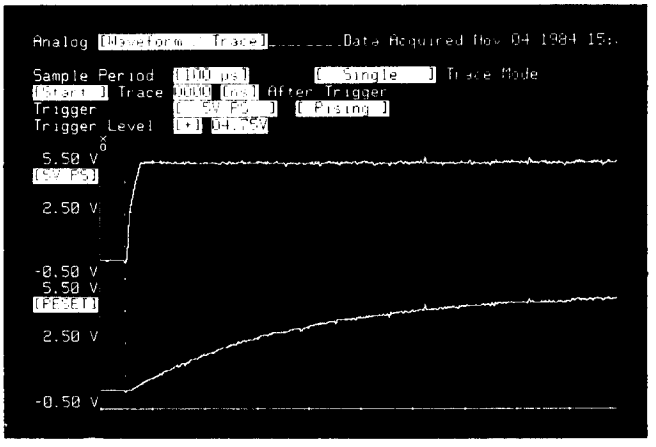


Figure 4

The tracepoint is shown at the left portion of the screen as a vertical dashed line. Notice that, at first inspection, the trace point doesn't appear as though it is at the 4.75 V trigger level we set for channel 1. Let's magnify the trace to see. Make sure the cursor is in the [Waveform/Trace] field, and press the NEXT[] or PREV[] key. This brings up the analog waveform diagram to allow more detailed analysis.

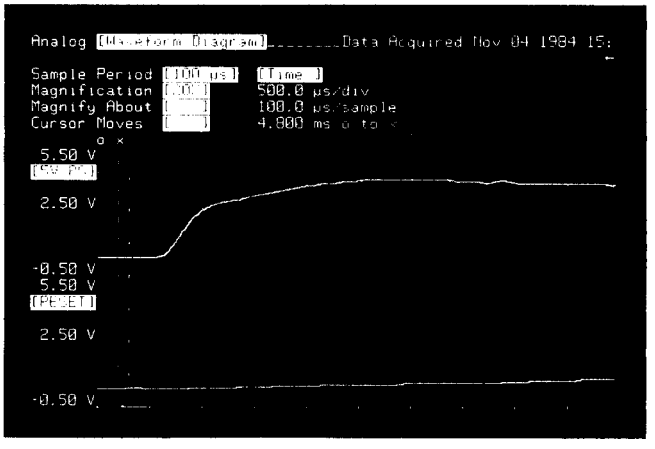


Figure 5

Using the CURSOR keys, move the cursor to the Cursor Moves field. This specifies which marker (x or o) can be moved along the waveform by the CURSOR keys. Again using the CURSOR keys, move the x marker to the tracepoint on the waveform, so we can magnify around the trace point. The HP 1631A/D always magnifies around one of the markers, as indicated by the Magnify About field. Move the cursor to the Magnification field and select [20X] with the NEXT[ ] key. Looking at the waveform, our previous suspicions seem to be confirmed. The trace point isn't on the rising edge of the power supply, let alone 4.75 V! Is the analyzer broken?

Obviously, it isn't, or we wouldn't have led you down this path. Instead, we are showing you a real advantage of a digitizing oscilloscope-the ability to trigger on events, even when it cannot display them due to a long sample period.

Change the magnification back to [1 X] and the sample period to 1 µs. Press the RUN key on the 1631 and cycle the power switch of the HP 5036A and capture another trace (be sure to wait two or three seconds between cycles to allow the power supply filter caps to discharge). You should have a display similar to that shown in figure 6.

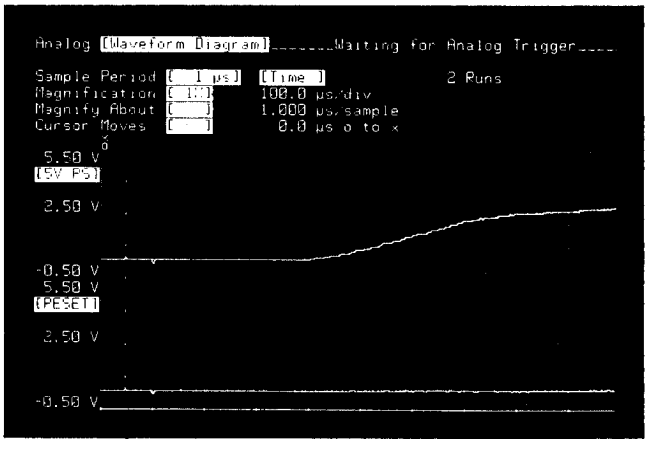


Figure 6

At the tracepoint, you see an excursion that the analyzer indicates is the first positive crossing of 4.75 V. Even at this sample rate, the analyzer may not display a spike that appears to go to 4.75 V. We chose this sample rate to show the beginning of the rising edge of the actual power up ramp.

For curiosity's sake, let's decrease the sample period to the minimum of 5 ns. Press the RUN key on the 1631 and cycle the power switch on the HP 5036A until the oscilloscope triggers. At this rate, you can readily see what the oscilloscope is triggering on, and we can also see that the excursions do cross our trigger level of 4.75 V.

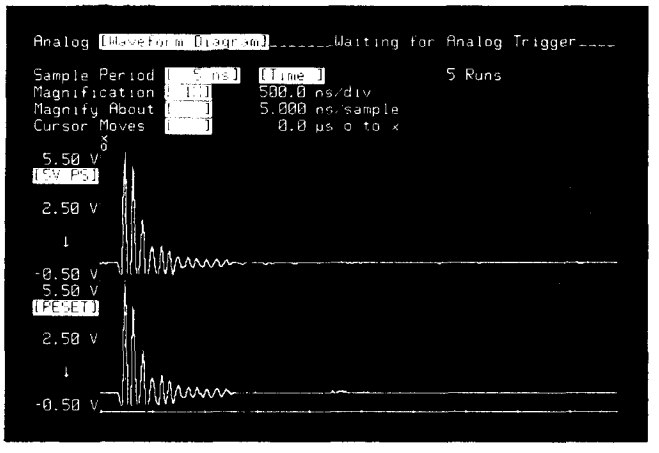


Figure 7

Conclusion: although the oscilloscope could not display the ringing before the supply ramped up, it told you that they were there by means of the tracepoint. By decreasing the sample period, we could capture and view the voltage spikes that were triggering the oscilloscope. It would be impossible to capture the same transitions with an analog storage oscilloscope and achieve this kind of viewing resolution. In the HP 1631A/D, this resolution is made possible by a 200 megasample-per-second rate.

Using The Digitizing Oscilloscope Within The HP 1631A/D (continued)

Measurement 3:
Using The Markers To Determine Time Intervals And Voltage Levels.

Problem: Measure from the time the +5 V power supply of the 5036A Microprocessor Lab reaches 4.75 V until the RESET line reaches 2.4 V (threshold).

Description: From the description given in measurement 2, remember that the period from when the +5 V supply voltage reaches 4.75 V until RESET crosses threshold must be at least 10 ms to ensure that an internal oscillator has stabilized. If the time is less than 10 ms, the manufacturer does not guarantee proper operation of the processor. An RC network consisting of a 3.3 μF capacitor and a 10kΩ resistor is attached to integrate the power up ramp applied to the RESET line. This should yield an RC time of 33 ms. But what is the actual time interval between the points in question? In this measurement we will use the markers on the waveform to find out.

Set up: To make the measurement we use the same trace specification as in measurement 2 with the exception of using single trace mode. Again we set the trace point to channel 1 (+5 V power supply) and 4.75 V on the rising edge. Even though we know the scope will trigger before the actual power supply ramp, you'll see that it will provide a good starting point.

Connect channel 1 to pin 40 of the 8085 and channel 2 to pin 36.

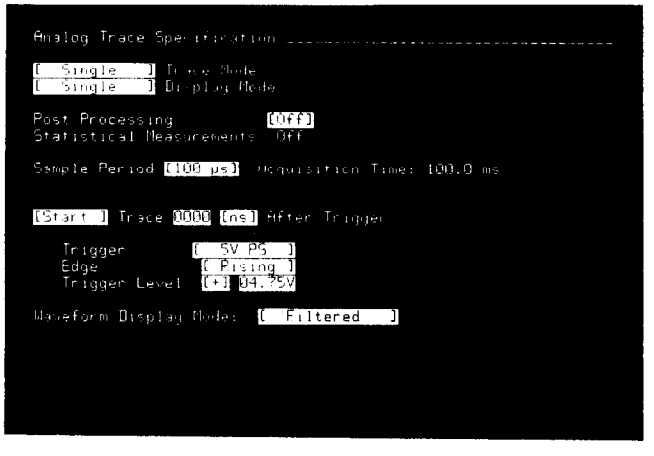


Figure 8

Turn the pow-er to the 5036A off, and press the RUN key on the 1631 Turn the 5036A power on, and note the waveform. It should look similar to the one we captured in measurement 2.

Note: *rhe +5 V power supply in some HP 5036As may nor reach 4. 75 volts. If you have one, change rhe trigger* voltage **for** channel *1* **of** *rhe 1631 to 4.5 volts. This is not rhe voltage specified by the manufacturer, but will still serve to illustrate the poinr.*

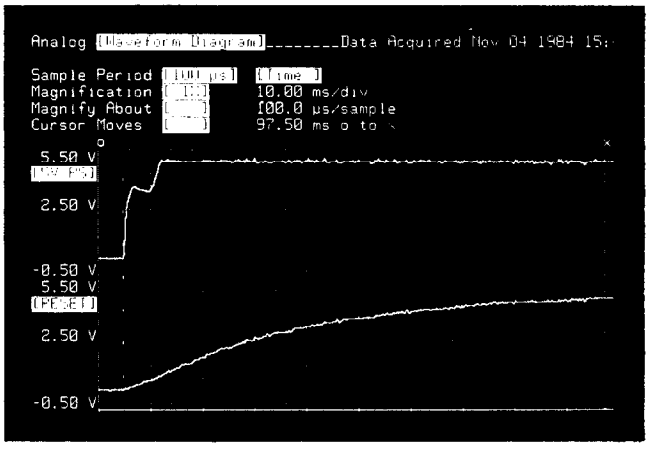


Figure 9

If your 1631 shows the [Waveform/Trace] display, move the cursor to the [Waveform/Trace] field and use the NEXT[] key to select the [Waveform Diagram] display. As you may recall from the previous measurement, this display allows us to use the markers on the waveform and to expand the display. Move the x marker to the trace point (the bright vertical dashed line at the left of the display). Change the Magnify About field to [x] and select Magnification [2X]. If the trace point is too far to the left of the screen, you can use the SHIFT and ROLL keys to move the waveform closer to the center of the screen. Now that the waveform is expanded, it will be easier to see where to move the x and o markers.

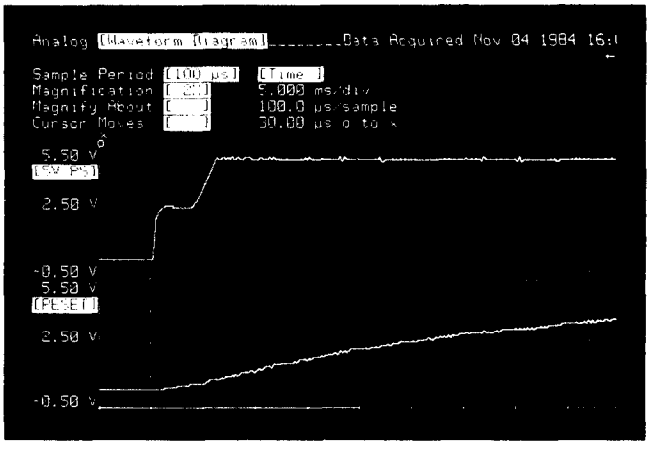


Figure 10

Move the cursor to the [Time] field and change it to [Volts]. This field specifies what the markers will read— time intervals or voltages. Since we want to find the time interval between two channels, we will start with the x marker on the power supply ramp at the 4.75 volt point. As the x marker is moved, notice that the voltage is displayed on screen. The field to the right of the volt/time field is used to select the channel the markers are reading.

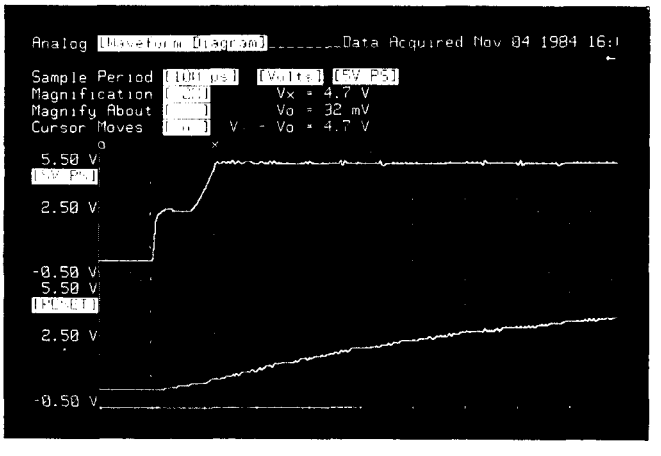


Figure 11

Keposition the cursor to this field and change the channel to RESET with the NEXT[ ] or PREV[ ] key. Change the Cursor Moves field to [o] and move the o marker to the 2.4 volt level on channel 2, as shown in figure 12.

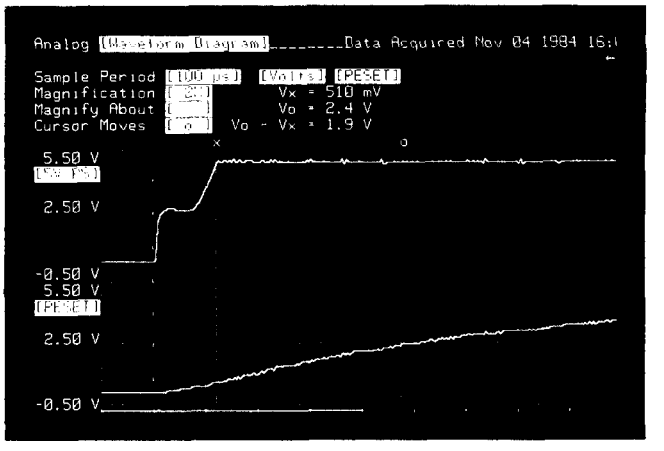


Figure 12

Change the marker function back to [Time] and read the time displayed from the x to o marker. Making a time interval measurement based on voltage is that easy! We can see in figure 13 that the time margin is well within the specifications given by the manufacturer.

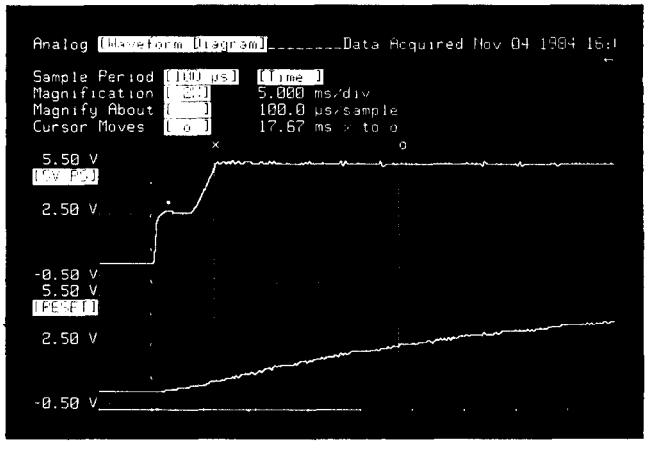


Figure 13

Conclusion: Use of the markers in the digital oscilloscope make time interval and voltage measurements an easy task. This is especially important when a time interval is critical in a design.

Using The Digitizing Oscilloscope Within The HP 1631A/D (continued)

Measurement 4:
Using Analog Post-processing To Mark Events.

Problem: Measure from the time the +5 V power supply of the 5036A Microprocessor Lab reaches 4.75 V until the RESET line reaches 2.4 V (threshold) in a continuous trace mode. If the time is less than the 10 ms the manufacturer requires, stop the analyzer. Otherwise, develop statistics on the time interval and display the maximum and minimum.

Description: The two previous measurements have concentrated on measuring the time interval from when the +5 V power supply reaches 4.75 volts at power up to when the RESET line reaches 2.4 volts. Since the manufacturer specifies that the time must be at least 10 ms, we want to check the RC integrator on the RESET line to make certain that the time constraint is not violated. If the time is ever less than 10 ms, we want the scope to stop and capture the violation. But even if the time is not less than 10 ms, we would like to gather some statistical information about the time interval, specifically the minimum time.

In this measurement, we will use another powerful feature of the digitizing oscilloscope in the 1631—post processing. The post processing feature has two parts, post acquisition triggering and statistical measurements.

Post-acquisition triggering is a sort of triggering after the fact. When we set trigger and trace specifications for the scope, we are qualifying data to store in memory. This data is then displayed on screen. Post processing allows us to tell the 1631 to check for specific events in the acquired data. If these events occur, the 1631 will record a "hit", and stop if it is in single trace mode, or make another acquisition if in continuous. If in continuous trace mode, the number of runs (acquisitions) is displayed on screen as well as the number of hits (post acquisition events).

The 1631 is also capable of displaying statistical information about the hits in memory, like the maximum and minimum time between events or the mean time and standard deviation of the events.

Last, but certainly not least, we can cause the 1631 to search the acquired data for an event and stop if it finds one. This is an important capability because in certain cases it may be necessary to look at the data that led to that event. By stopping the analyzer when the event occurs, we have captured data leading up to it. You can use this capability as a sort of baby sitter to capture the desired event.

We use essentially the same trace specification as in the previous measurement, with two basic changes. First, we will change the trace mode back to [Continuous]. Second, we will turn the Post Processing and Statistical Measurements fields to [On]. When the Post Processing field is changed to [On], notice that a bracketed field appears at the top of the trace specification menu, labelled [Trace Specification]. This field allows you to select the analog trace specification menu (that we have used in the last two measurements) or a post processing trace menu.

Set up: Connect channel 1 probe to pin 40 of the 8085 and channel 2 to pin 36. Press the TRACE key and set the trace specification as shown.

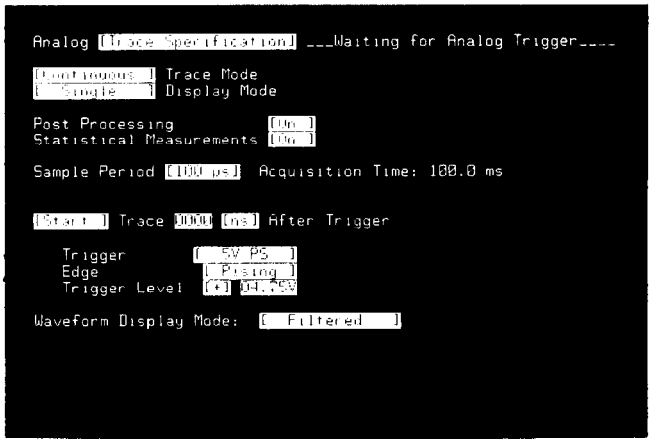


Figure 14

After the trace specification is set as shown, press the TRACE key again (this moves the cursor to the top field in the menu; neat, huh?). Press the NEXT[] or PREV[] key, which puts you into the post processing trace specification menu. Change the post processing menu to match the one shown.

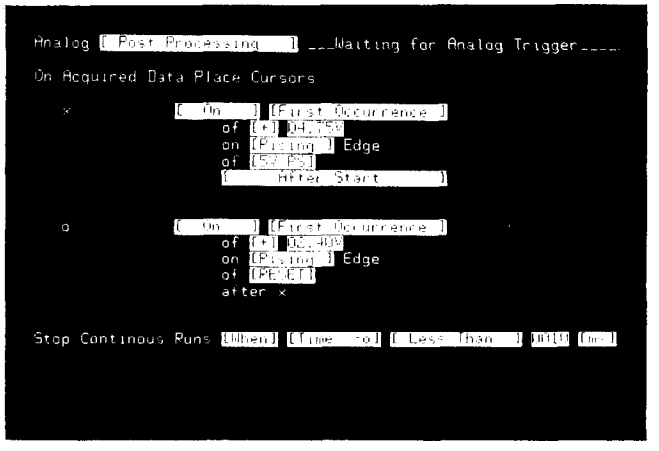


Figure 15

What does this all mean? We have just told the 1631 to look through the data it will capture and place the x and o markers as shown. In other words, after every acquisition the 1631 will check for the first rising after the trace point which goes through 4.75 volts on the +5 V power supply (channel 1). It' it finds one, the x marker will be placed on that point. It will then look for the first occurrence of a rising edge going through 2.4 volts on the RESET line (channel 2). If it finds one, it will place the o marker on that point. If both of these events occur in one acquisition, a hit is recorded and the analyzer starts the next acquisition, If they do not occur, or if only one occurs, the analyzer does not record a hit and it starts the next acquisition. Notice the field at the bottom of the menu. This tells the 1631 to stop its continuous trace mode if the time between event x and event o is less than 10 ms. When set, the analyzer will stop should it ever encounter an acquisition when the time between the 4.75 volt point of the +5 V power supply, and the 2.4 volt of the RESET line is less that 10 ms. It could also be set to stop should the time exceed 10 ms, but that would make no sense for this measurement. If the 5036A was designed properly, this event (10 ms) will never occur.

Note: us *with* ***measurements 2 and 3, you may encounter a 5036A + 5 V power*** *supply that* ***does not*** *reach* ***4.75*** *volts.* ***If this is rhe case, change*** *the trigger* ***and post-processing level for channel I to 4. 5 volts. Even though this*** is ***nor the*** *voltage* ***specified by*** *the manufacturer,* *it* ***will*** *still* ***serve*** *to illustrate our point.*

Press the RUN key on the 1631 and cycle the power switch on the 5036A a number of times. The 1631 will probably trace on the power up and power down portions of the cycle, since at power down there well may be transients that meet the trace specification. You should also notice that the 1631 shows the number of runs and hits in the upper right of the display. Remember that "runs" is the number of times that the trace specification is met (in other words, the number of acquisitions) and "hits" is the number of times the post processing specification is met.

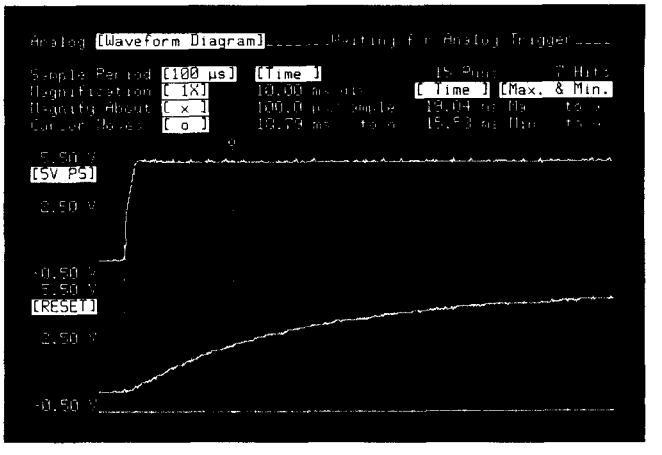


Figure 16

The field below the number of runs should display [Time]. When in the time display, the field to the right of it (under the number of hits) is used to select the statistical information. You can select [Max. & Min.] or [Mean & Dev.]. The max and min display tells the minimum and maximum times encountered between the specified post processing events. Change the field back to [Max. & Min.].

Change the [Time] field discussed above to [5V PSx]. The screen now displays the maximum and minimum values encountered for channel 1 (5V PS) at the x marker. Since this was specified in the post processing menu, the maximum and minimum values should be the same. You can use this field to get information about both markers on both waveforms. Cycle through them and observe the ranges possible.

Conclusion: Post processing of the analog channels in the 1631 allow you to gather time interval statistics for verification of design criteria, as well serve as a babysitter for critical events. If such an event should occur, the analyzer can be instructed to stop, while having captured the data that led to it.

Using The Timing Analyzer Within The HP 1631A/D

In this section of the guide, we will use a new target system as part of the HP 5036A microprocessor lab. It is an extension memory board that plugs directly onto the edge connectors of the HP 5036A and provides an additional 64k of memory. Even more important than the memory size, however, is the type of memory used. Dynamic RAM (DRAM) was chosen for a number of reasons. First, DRAMs are bring designed into an ever increasing number of new projects. Second, because of timing and other constraints, they present some unusual and sometimes frustrating problems not often encountered in static memory designs. A number of these problems are addressed directly by the feature set of the HP 1631A/D, as you will see in subsequent measurements. Third, even though the HP 5036A is not a state-of-the art microprocessor design, the concepts used to address the DRAMs here are a subset of those used in all microprocessor systems that incorporate DRAM.

The challenge in designing with DRAMs is to make them appear as static RAM to the microprocessor. This is often easier said than done. A DRAM controller chip on the board (i.e., a National 8409) makes the task much easier and more predictable. It accepts a few signals from the processor and generates the necessary control and clock signals for the DRAMs.

Before plugging the DRAM board onto the edge connectors of the 5036A, you will need to cut trace J 1 near the 8085 processor. This enables the DRAM board to exercise the HOLD line when needed. Once this trace is cut, it will be necessary to reinsert a jumper into J1 if the 5036A is to be used without the DRAM board. If the jumper is not inserted, and the DRAM board is not connected, the 5036A may not work.

If you have not had exposure to memory systems in general and DRAM systems in particular, we suggest you go through Appendix A and get some exposure to the theory behind the DRAM board. This will make the timing analysis section much more meaningful.

Introduction to Timing Analysis

Before we delve into the second portion of the HP 1631A/D, a brief discussion of what a timing analyzer is would be in order.

First, what is a timing analyzer? As digital circuits and microprocessors developed in complexity through the late 1960s, and early 1970s, it became ohvious that oscilloscopes had a number of shortcomings for testing these circuits. First, there were usually eight to 16 lines that were of interest in a bus ‘structure from a microprocessor, and the designer needed to know what was occurring on all at the same time. Oscilloscopes simply did not have enough channels. Second, the designer often wasn’t as concerned about the actual waveshape as when the signal crossed the logic threshold to become a 1 or 0. It was also necessary to know the relationship of these signals in to time. Thus, there was a need to trigger on a particular pattern of levels on all of the lines (we refer to this pattern triggering or pattern recognition). In some cases a list representation of the waveforms with 1s and 0s was also extremely helpful. An oscilloscope could trigger on one input, but not a combination of many inputs at the same time, and it certainly couldn’t generate a list of Is and 0s. Last, it was sometimes necessary to look at the patterns on the chosen lines before the trigger pattern, perhaps to determine what may have caused an error in xubsequent patterns.

Using The Timing Analyzer Within The HP 1631A/D (continued)

Out of these needs came the timing analyzer. Like the oscilloscope, the X-axis was time and the Y-axis, voltage. Unlike the oscilloscope, however, the data was sampled asyncronously and had a number of channels for checking a bus structure. To the timing analyzer, only one voltage is of concern-the threshold. Everything above the threshold is a high or 1, while everything below is a low or 0 (assuming positive logic). It is important to remember that the timing analyzer is not intended to make parametric measurements; that is the realm of the oscilloscope. By the same reasoning, the oscilloscope is not an effective tool in the realm of timing analysis. Each has its own strengths.

The timing analyzer in the HP 1631A/D allows you to trigger on not only levels, but on edges or a combination of the two. It can trigger on glitches; a glitch is any signal that crosses the logic threshold twice between sample periods of the analyzer. A valid pattern duration can be set that specifies a period of time for which the set pattern must be true in order for the analyzer to recognize it as valid. Timing can be shown in a list, which often makes it easier to follow complex patterns.

We will explore these capabilities in this section, and attempt to take some of the mystique out of timing analysis. Since it is in the same domain-time-as the oscilloscope, it is really a fairly easy tool to learn to use effectively.

Measurement 5:
Using The Timing Analyzer To Capture And Display Some Of The More Important Signals On The DRAM Board.

Description: as was mentioned in the introduction to this section, a timing analyzer has many advantages over an oscilloscope when looking at a number of digital signals with the need to trigger on a particular pattern. In this case, parametric information is not needed, as we are concerned only with the timing of the signals.

Set up: connect the lines of pod 0 (timing pod) to the points listed below on the DRAM board. Use the grabbers provided with the HP 1631D clip onto the points listed below.

Pod 0 Bit	DRAM Board Connection Point	Signal Name
0	U9 8409 pin 1	RFCK
1	U9 8409 pin 28	RAS
2	U9 8409 pin 32	CAS
3	U9 8409 pin 46	RFREQ
4	U9 8409 pin 5	RFRSH
5	U9 8409 pin 2	RGCK

Since you will be using the timing analyzer, you must set the system configuration as shown in figure 17. The system configuration menu is reached by pressing the SYSTEM key, which is one of the six along the top of the keyboard. Change the configuration using the ROLL keys.

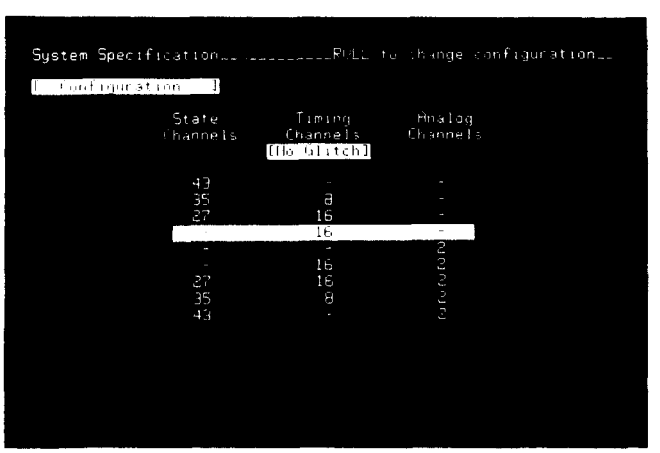


Figure 17

Press the FORMAT key and configure the format menu to match the one shown in figure 18.

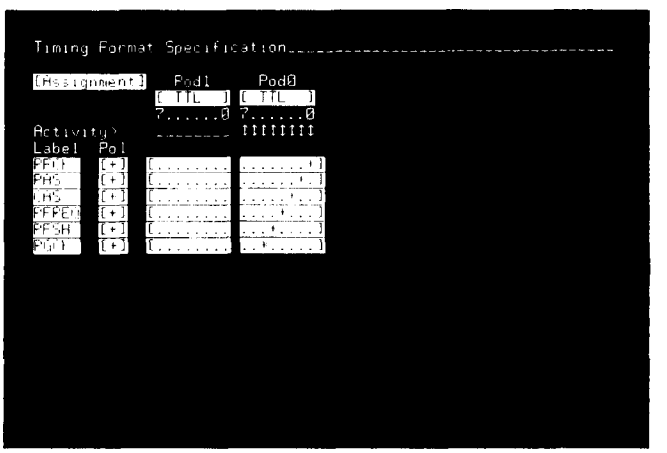


Figure 18

Everything is now set except the tracepoint. Press the TRACE key and set the trace as shown in the example trace menu figure 19.

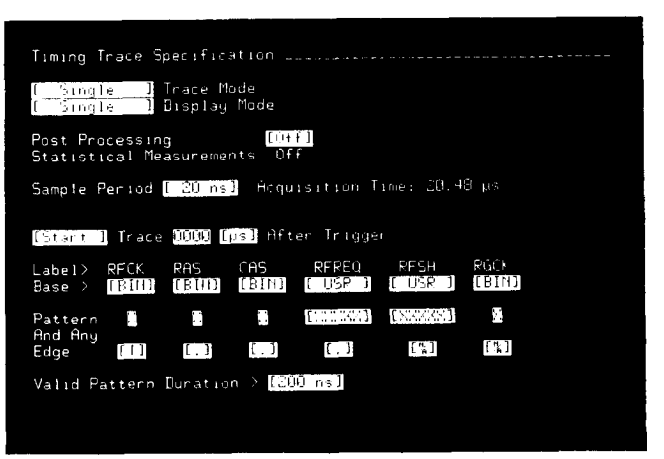


Figure 19

‘Using The Timing Analyzer Within The HP 1631A/D (continued)

The tracepoint tells the analyzer to look for an occurrence of a negative transition of RFCK and don’t cares on all of the other lines. This allows us to capture the second portion of the refresh cycle for the DRAMs. Recall from the overview in Appendix A that in our DRAM system, if a hidden refresh has not occurred during the rime that RFCK is high, the 8409 DRAM Controller requests that the microprocessor suspend operation (HOLD) while it refreshes the current row in all of its DRAMs. If a hidden refresh has occurred, the 8409 does not issue a HOLD request. In the case that a hidden refresh has not occurred, our trace should show RFCK going low and RFREQ (pin 5) going low a maximum of 30 ns later. Some time after that, the HOLD should be acknowledged by the microprocessor through pin 46 (RFSH) of the 8409 and. it will proceed with the forced refresh.

In the case that a hidden refresh has occurred while RFSH was high, a flag is set internally in the 8409 to tell it that a forced refresh is not needed. Consequently, when RFSH goes low, the DRAM controller continues with normal operation.

On the 5036A, enter the following keystrokes:

```
FETCH ADDR
8000
C3
STORE/INCR
00
STORE/INCR
80
STORE/INCR
FETCH ADDR
8000
RUN
```

This short program gets address 8000 in DRAM, stores address 8000 as the jump address, and jumps back to itself. In other words, it continually loops back to address 8000. Since this address is in DRAM, it should cause a forced refresh, because the 8409 will never detect the microprocessor trying to access something else. The 8409 never finds time to slip in a hidden refresh.

Press the RUN key on the HP 1631.

With the trace specification that we have set, we should capture one of the two sequences listed above. The first case (forced refresh) is shown in figure 20.

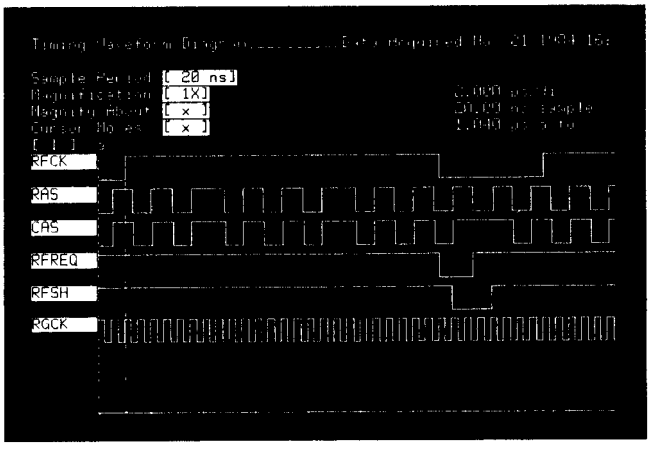


Figure 20

Press the RESET key on the HP 5036A. This puts the 5036A back into the keyboard monitor routine. Since it is monitoring only keyboard presses and not accessing DRAM, hidden refreshes should occur all the time. Press the RUN key on the HP 1631.

The second case, that of a hidden refresh is shown in figure 21.

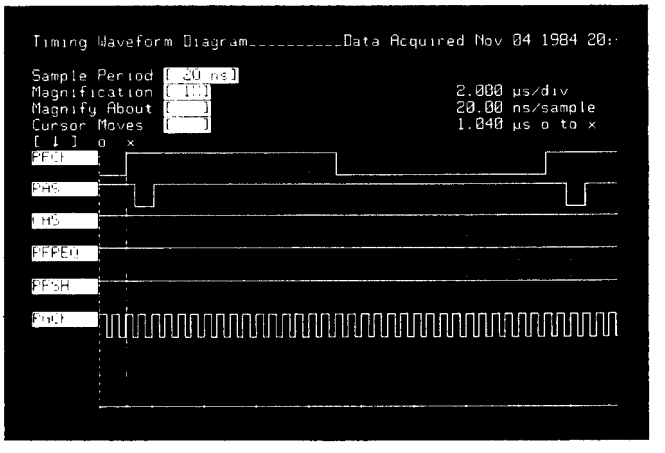


Figure 21

Notice that the tracepoint in both diagrams and on your analyzer is at the left hand portion of the screen. It is represented by the heavy vertical dashed line. Now suppose we want to see more of what occurred before the actual tracepoint (negative time). Press the TRACE key and set the tracepoint to [Center]. Press the RUN on the 1631 to capture new data with the trace point at center. The tracepoint should now appear at the center of the screen with data before and after it.

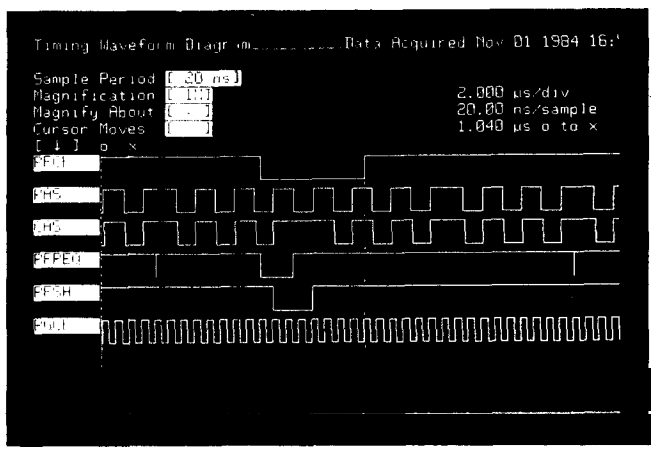


Figure 22

If you set the tracepoint at [End], the tracepoint will be at the right side of' the screen with all of the events before the tracepoinr displayed to the left.

Change the trace point back to [Start].

As mentioned earlier, it is sometimes helpful to display the timing information in a list form in addition to the waveform display. If you press the LIST key, which is one of the six along the top of the keyboard, a list representation appears of what is on-screen. Notice that you can shift from the trace specification, to format specification, to waveform diagram, to list representation by pressing one of the six: keys along the top of the keyboard. These keys represent the major functional areas of the analyzer, although some are not appropriate for certain operations.

In the list mode, all of the data is listed as a 0 or 1. This is appropriate, but suppose we would like some labels, other than 1 and 0, that are more descriptive of what those two numbers represent. Let's use an example. In the case of RFREQ (REFRESH REQUEST), when the signal is low, a forced refresh is requested. When the line is high, a forced refresh is not requested or the system is looking for a hidden refresh. So instead of 0 and 1 in the list, it would be clearer to display them as RFREQ, and IDLE, respectively. By the same reasoning, we could label the 0 and 1 states of RFSH as FRFSH (for forced refresh) and IDLE, respectively. Press the FORMAT key and move the cursor to the [Assignment] field. Press the NEXT[] or PREV[] key to enter the [User Base] menu. Notice that for each of the signals previously defined in the format menu, there are two highlighted blocks representing 0000 and 0001. The number of blocks is determined by how many bits were set in the assignment menu. In each case, we defined only one bit for each signal. That gives two possible states, (on or off) for each. Consequently, there are two highlighted blocks shown for each of the signals. Even though there are two states for each signal, these states can be labelled anything you like. This allows you to assign labels that are more meaningful to the particular signal than just ON and OFF, or 1 and 0.

Position the cursor and enter the labels as shown from the keyboard.

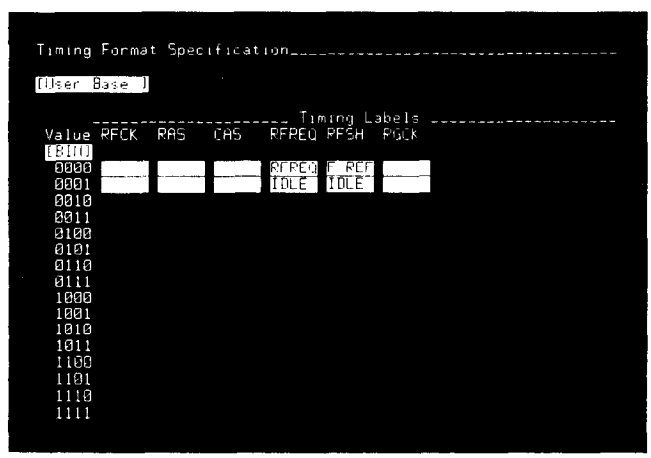


Figure 23

Press the LIST key and move the cursor to the Base field below RFREQ. Using the NEXT[] or PREV[] key, cycle through the choices until (USR] is displayed. This is the user-defined base. Do the same for RFSH and look at the list. All of the 0s and 1s have been replaced with the names you entered into the user base. Notice that the measurement does not have to be re-run. This feature makes a list much easier to read and eliminates the need for you to recall exactly what each state means for each labeled signal. User base accepts signals with up to 4-bit lengths, as assigned in the format [Assignment] menu, for a possible list of 16 states for each signal. Each of these 16 states can be labeled with a descriptor, as was done with the two states of RFREQ and RFSH.

Using The Timing Analyzer Within The HP 1631A/D (continued)

There are several other advantages of the list format. Suppose you want to look for a unique pattern that represents a forced refresh in your data. One way to find it would be to look at the timing diagram and check the state of each line until you found what you were looking for, assuming that it happened within your acquisition. An easier way is provided in the list mode. During forced refresh, we know that RFCK, RFREQ, and RFSH are all low. This indicates that the refresh clock (RFCK) has gone low, that a forced refresh request (RFREQ) has been issued to put the microprocessor in a HOLD state, and that the refresh has been acknowledged (RFSH) by the processor, saying that it is in HOLD state while the 8409 refreshes the RAMs. Press the LIST key and position the cursor in the [Mark] field. To the left of the

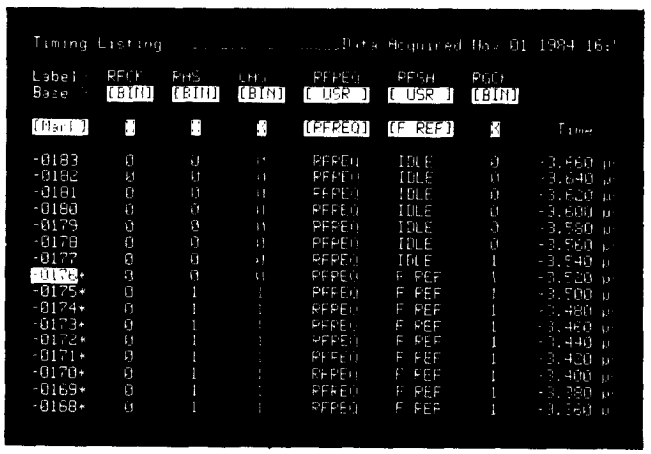


Figure 24

[Mark] and under each signal name, there is a field that has an X for Don't Care in it, or in the case of the two signals we labeled, RFSH and RFREQ, there is a bracketed field with several Xs. These allow us to tell the analyzer to search its data for a unique pattern. Move the cursor to the field under RFCK and enter a 1 from the keyboard. Now move the cursor to the same fields under RFREQ and RFSH and using the NEXT[] key, cycle through until the analyzer displays RFREQ and FREF in the fields. All occurrences of that pattern are now marked with an "*" next to the memory location at the left of the screen. We could scroll through the whole memory with the ROLL keys to find all of those occurrences, but it is unnecessary. Move the cursor back to the [Mark] field and press NEXT[]. The field displays [Show], and the list displays only those occurrences of the unique pattern you requested.* Using the ROLL keys, scroll down in the list. Press the WAVEFORM key and notice that the point you were in in the list is marked on the waveform with the X marker. You have found the occurrences of a forced refresh on the waveform using the list format.

****If the analyzer doesn't display anything, it means that it didn't capture a forced refresh cycle. You may want to press the RUN key until one is captured.***

Conclusion: with very little pain, you have used the timing analyzer to capture and display some of the more important control signals on the DRAM board. The waveform display allowed you to see the signals as they related to each other in time without unnecessary parametric information. You also saw the information in a list format and learned to put more meaningful information into it than 0s and 1s. When you are concerned about time sequences of hardware events, the timing analyzer gives you a lot of information with little visual clutter. It also gives you negative time, which allows you to look at data before the specified tracepoint. This was exemplified when you set the tracepoint to be displayed in the center of the screen, rather than at the start.

This measurement was intended to give anyone who has not used a timing analyzer some familiarity with one and to build confidence that there really isn't any magic in logic analyzers. When compared to an oscilloscope, a timing analyzer is an extension that allows you to deal with a different set of problems. The next few measurements cover some actual design concerns in DRAM design and show how the feature set of the HP 1631A/D is suited to the hardware designer's needs.

Measurement 6:
Using The Timing Analyzer And Post-processing To Determine Maximum Forced Refresh Time.

Description: The 64k DRAMs on the board have a maximum refresh time of 2 ms. The RAMs have 128 rows x 512 columns, internally. All memory cells in a row can be refreshed by accessing that row with a RAS pulse. So, to refresh the whole KAM, all 128 rows must be refreshed within the 2 ms cycle time. The amount of time spent on each row is then 2 ms/128 rows = 15.6 μs, or 16 μs to round off. This time is the period of the clock given to the 8409 DRAM controller at pin 1 as the refresh clock (RFCK). Using either hidden or forced refresh, the row the controller is accessing must be refreshed within that 16 μs. Hidden refresh is allowed on the positive portion of RFCK. When RFCK goes low and if a hidden refresh has not occurred, the 8409 initiates a forced refresh. The problem with forced refresh is that the 8409 must request that the system processor suspend all exterior operations while it refreshes the RAMs. The processor is then essentially idle during this time. How long is this time? According to the 8409 data sheet, a forced refresh takes approximately four cycles of the system clock, or in the case of the 5036A with a 2 MHz clock: 500 ns x 4 = 2 μs. Since, in worst case, this 2 μs forced refresh could happen every cycle if a hidden refresh can't be performed, the processor could be idle as much as 2 μs/16 μs = 12.5% of the time. In many cases, this might clearly be unacceptable. What to do!

Luckily, there is nothing to prevent us from making the clock asymmetrical to allow more time for a hidden refresh to occur. Remember from our discussion in Appendix A that the 8409 looks at the chip select line and slips a hidden refresh in whenever the processor is accessing something besides its DRAMs. By lengthing the time that RFCK is high, we are creating a greater probability that the processor will access something other than RAM, and a hidden refresh can be performed. But we need to know the time that it really takes for the processor to react to a forced refresh request, since that impacts how long RFCK can remain high.

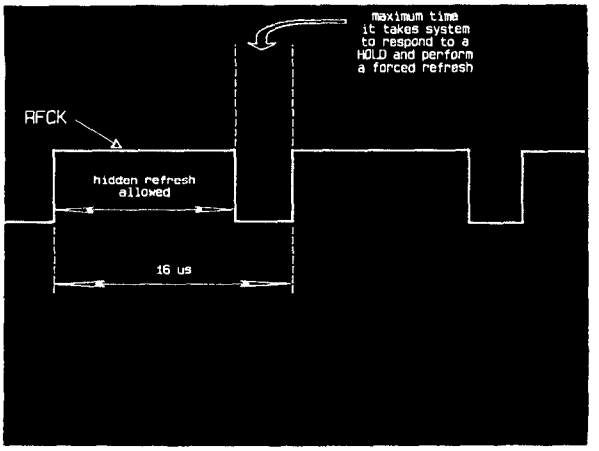


Figure 25

We will use the post processing capability of the timing analyzer to determine the maximum time it takes for the processor to respond to a HOLD request from the 8409, added to the time it takes the 8409 to perform a refresh.

Set up: the DRAM board has a switch that allows a symmetrical or asymmetrical clock. Since we want a symmetrical clock, make certain that S1 is in the open position.

Use the same physical connections to the system as was used in measurement 5.

Use the same format specification as in measurement 5.

What point should we set the analyzer to trace on? First, let's determine the start of the cycle. Clearly, the next cycle starts when RFCK goes high. Set the trace specification as in figure 26.

Using The Timing Analyzer Within The HP 1631A/D (continued)

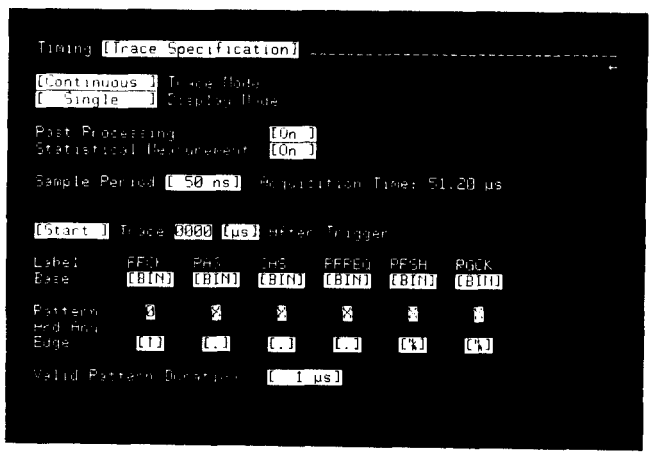


Figure 26

Post-processing in timing allows us to do functions similar to those in analog. We want to set up a post-processing specification that allows us to measure the actual refresh time. To get to the post-processing menu, press TRACE and set the post-processing and statistical measurement fields to [On]. Press the TRACE key once more to place the cursor at the top of the screen, and then move the cursor to the right to the field labelled [Trace Specification]. Press the NEXT[] key. Set the post-processing specification menu to match the one shown.

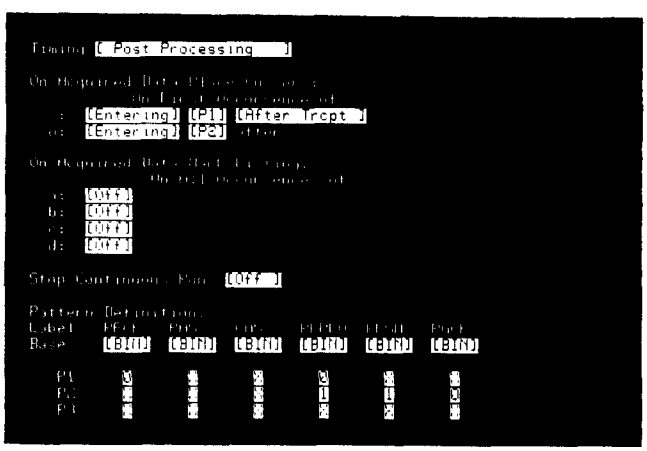


Figure 27

This post-processing specification tells the analyzer to measure the time between entering a pattern of RFSH going to 0 (the 8409 getting a hold acknowledge from the processor) and entering a pattern of RFSH = 1 (hold acknowledge ended), RFREQ = 1 (hold request ended), and RGCK = 0 (the end of the refresh cycle, per the 8409 data sheet). RGCK is the same as the system processor clock, and when it goes to 0 after RFREQ and RFSH have gone to 1, the processor is starting a new cycle after being held off.

Press the FETCH ADDR key on the 5036A and enter the following program into the 5036A.

FETCH ADDR
8000
C3
STORE/INCR
00
STORE/INCR
80
STORE/INCR
FETCH ADDR
8000
RUN

This program, which we used before, forces the DRAM board into forced refreshes, so that we can measure exactly how long they take. Press RUN on the 5036A and on the HP 1631A/D. Let the analyzer run for a minute or so and observe the minimum and maximum numbers on screen. You should get a maximum somewhere around 2.75 µs (figure 28). What does that mean?

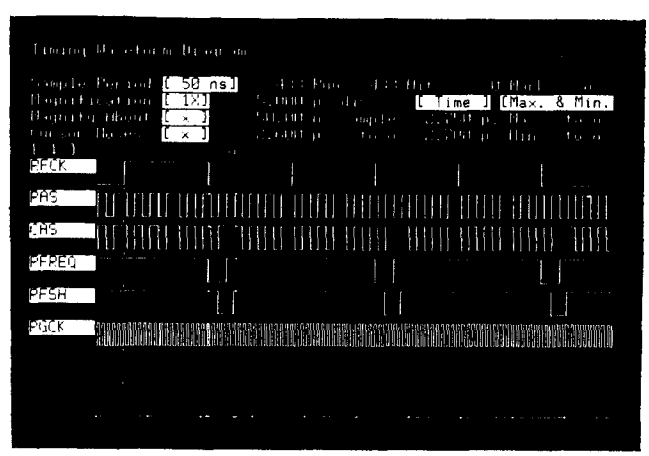


Figure 28

It means that the low period of RFCK can be changed to 3 μs, allowing an extra 5 μs for a hidden refresh to occur. How does this affect our processor overhead? Our old figure indicated that the processor's idle time was 12.5% worst case, based on figures in the 8409 data sheet. But we now have some empirical data to recalculate worst case overhead. If the system's idle time is 2.7 μs out of a cycle of 16 μs, the processor is actually idle 16.9% of the time. We now know that our processor should not be idle more than 16.9% of the time.

Conclusion: using the post-processing features of the HP 1631A/D, we were able to gain empirical data about our system that was more appropriate than average calculations. In many cases, event-driven time interval measurements, like those provided by post-processing in the HP 1631A/D, may allow you to time-characterize parts of your system that would be Impossible to make calculations on.

Measurement 7: Using Timing Post-processing To Determine Actual System Overhead For Refresh

Description: in the last measurement, we used timing post-processing to determine the maximum time needed for a forced refresh. This time was in turn used to determine how we could make our system more efficient by increasing the possibility of a hidden refresh. In this measurement, we will again use timing post-processing to determine how much an asymmetrical clock can lower system overhead in actual operation. In measurement 6, we forced the system to perform forced refreshes on every cycle so we could measure how long it took. In normal system operation, at least some hidden refreshes occur. We would like to make measurements to determine the actual idle time of the processor by finding out how many forced refreshes occur in operation. Since there is no way of calculating this, we must rely on a measurement.

We know from previous measurements that the percentage of overhead is given by the hold time per cycle divided by the time per cycle or hold time/cycle time. To find the total overhead, we must know the ratio of forced refreshes to total number of refreshes. The total system (overhead percentage for forced refreshes should be the product of these two, or:

$$\text{total system overhead } \% = \frac{\text{idle time/cycle}}{\text{refresh cycle time}} \times \frac{\text{number of forced refreshes}}{\text{total number of cycles}}$$

'This may look complex, but it really is quite simple. We are looking for the percentage of a cycle that a forced refresh takes. Secondly, out of a given number of cycles, how many are forced refreshes in normal operation? The product of the two represents the percentage of time the processor spends idle in normal operation. This percentage can just as easily be found for a symmetrical or asymmetrical clock. The percentages can then be compared to see how much of a reduction in system overhead an asymmetrical clock makes.

Setup: we will use two features of timing post-processing to help us calculate these percentages. The first was used in measurement 5. The second, which we will use now, is called marking.

All physical connections to the system are the same as in measurement 5.

Switch S 1 on the DRAM board determines whether the refresh clock RFCK is symmetrical or asymmetrical. Since our first measurement is based on a symmetrical clock, make certain that S1 is in the open position.

The format specification is the same as in measurement 6.

Use the same trace specification as measurement 6.

The post-processing menu should reflect the one shown in figure 29.

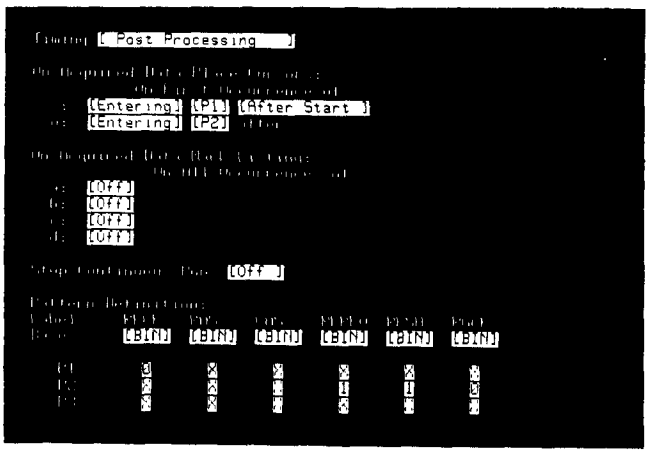


Figure 29

In the trace specification menu, the analyzer was set to trace whenever a new refresh cycle started, which is every 16 μs. On the timing diagram this number is the "Runs" column. This tells us how many times the trace specification was met and the analyzer captured data. Whenever the trace specification is met, the post processing menu checks the data in memory. In post-processing, we will first set a specification that tells how many forced refreshes occurred. Remember that the first event in a forced refresh is the RFREQ (REFRESH REQUEST) line pulled low. When the post-processor sees this condition in the acquired data, it records it on the timing diagram as a "hit." If we incorporate these two bits of information from the timing diagram into the formula we developed before, we get:

$$\text{total system overhead } \% = \frac{\text{idle time/cycle}}{\text{refresh cycle time}} \times \frac{\text{number of hits}}{\text{number of runs}}$$

Since we know that the refresh cycle time is 16 μs, all that is needed to complete the formula is the idle time/cycle. Post-processing provides the mean and standard deviation of marked events, so we will use the mean to calculate the mean cycle time and the standard deviation to calculate our error.

Enter the following program on the 5036A.

```
FETCH AD DR
0800
00
STORE/INCR
41
STORE/INCR
42
STORE/INCR
41
STORE/INCR
00
STORE/ INCR
80
STORE/INCR
FETCH ADDR
4020
RUN
FETCH ADDR
8000
```

Press the RUN keys on the 5036A and the HP 1631A/D. Let the microprocessor lab run for a few minutes, then press the STOP key on the HP 1631A/D. Notice the field beneath the Marks x-o field. It should read [Mean & Dev.]. If it does not, use the NEXT[ ] key to change it. We now have enough information to complete our equation.

$$\text{total system overhead \%} = \frac{\text{mean x to 0}}{16\ \mu\text{s}} \times \frac{\text{number of hits}}{\text{number of runs}}$$

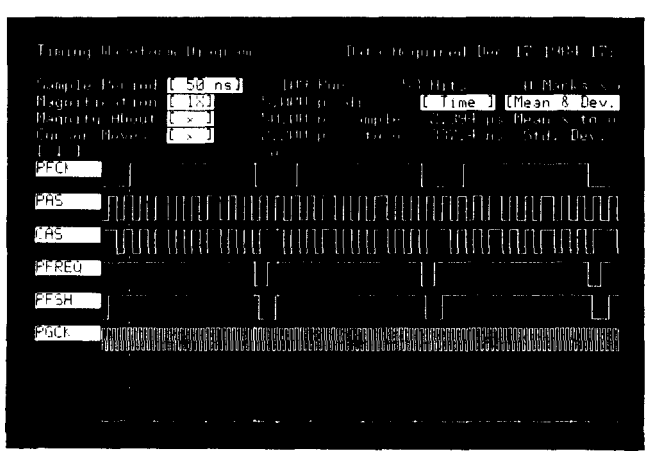


Figure 30

The number you get will probably differ from what is shown, but it should be in the same neighborhood. It represents the mean total percentage of time the processor spent in the hold state for that time.

Now change S 1 on the DRAM board to the closed position and rerun the measurement. To make an accurate comparison, the number of runs for the symmetrical clock and asymmetrical clock should be the same or close to the same.

Did you notice any difference between the first and second runs? This can be a significant improvement in a RAM-based microprocessor system.

Conclusion: efficiency of a system can be difficult to measure from a hardware standpoint. The unique capabilities of the HP 1631A/D allowed us to make a complex measurement in a short time. One comment on post processing should be made here: it takes the HP 1631A/D about 100 ms to post-process the acquired data, and so there is a "dead" time between acquisitions. In the measurement we just made, that means that as many as 6250 refresh cycles may go by between HP 1631A/D acquisitions. That is why the data acquired in post processing should be taken as a statistical measure only. As with all statistical data, the more the HP 1631A/D is allowed to acquire, the higher the confidence level on the results. That also means that if post-processing is used on a repetitive event with a period greater than 100 ms, it is likely that the HP 1631A/D will capture all events.

Using The Timing Analyzer Within The HP 1631A/D (continued)

Measurement 8: 'Triggering On Glitches

Description: glitches are sometimes the bane of hardware designers, and often the most difficult thing to capture. It seems that if you have a glitch occurring intermittently, you are never able to catch the waveforms that contain the glitches with a timing analyzer. The HP 1630A/D can trigger not only on edges, but on glitches as well. This capability is carried through to the HP 1631A/D.

To create a clock with a 16 μs period as is needed by the 8409 DRAM controller, we use a D-latch to divide the 2 MHz system clock down to 1 MHz, which gives a period of 1 μs. A 74LS193 4-bit binary up/down counter is then used to divide by 16 to give a period of 16 μs. Look at the clock generated trom this circuit (i.e., RFCK), and notice that there is occasionally a glitch in the middle of the pulse. What is causing this glitch?

Setup: make the following physical connections to the DRAM board.

Pod 0 Bit	DRAM Board Connection Point	Signal Name
0	U2 pin 6 (74LS193 pin 6)	Q2
1	U2 pin 7 (74LS193 pin 7)	Q3
2	U9 pm I (8409 pin 1)	RFCK

Make certain that S1 on the DKAM board is in the closed position.

Press the SYSTEM key and move the cursor to the [No Glitch] field. With the NEXT[ ] key, change it to [Glitch]. Notice that the number of timing channels is halved. When the HP 1630A/D was designed, there was a choice between halving the number of' channels or halving the memory depth, or reducing the sample rate in glitch mode; the former was chosen to provide maximum memory and sample rate.

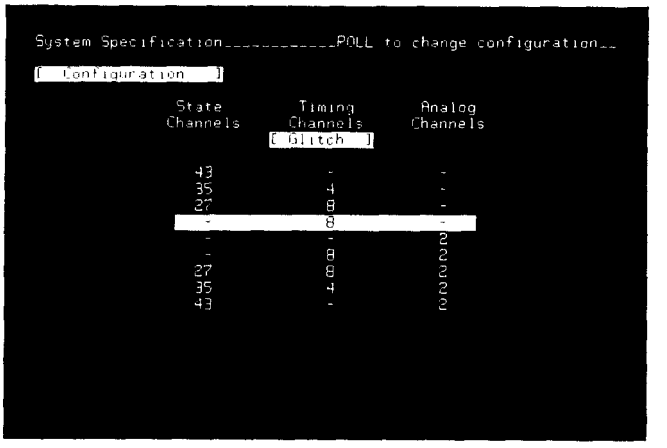


Figure 31

Press the FORMAT key and change the format specification menu to match the one shown in figure 32.

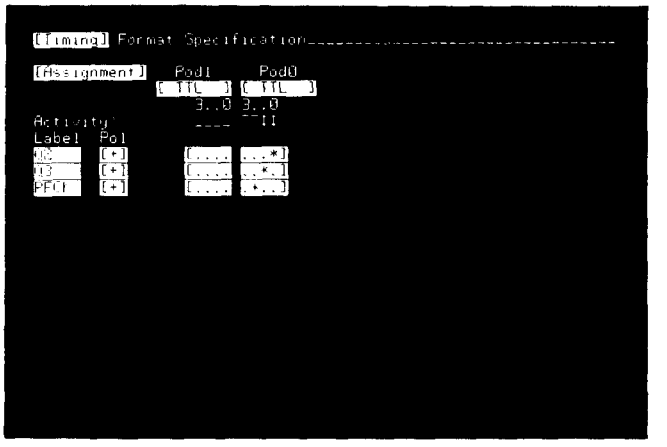


Figure 32

Press the TRACE key and change the trace specification menu to match the one shown. Notice that the glitch capability is enabled on all three lines. We will trace on a glitch on RFCK in the end trace mode. We chose end trace because we would like to look back at Q2 and Q3 to see what was happening on them when the glitch occurred (i.e., negative time capability). Remember, Q2 and Q3 are used to generate RFCK, and will happen before RFCK.

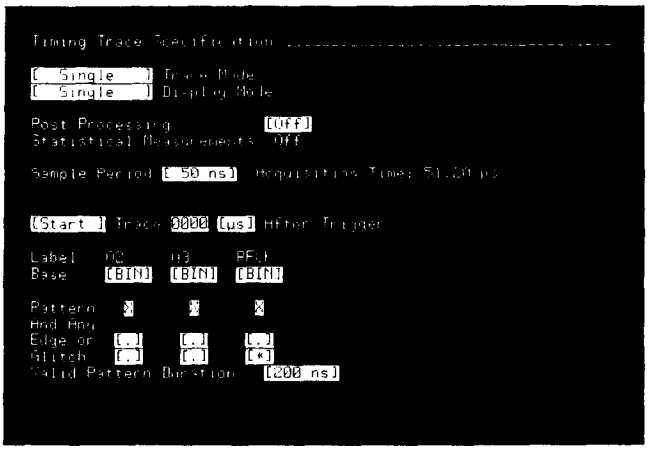


Figure 33

Press the RUN key on the 1631 and look at the display. The waveform should show a negative-going glitch on channel 3 at the right side of the screen. A glitch is represented by a bright dashed line on the waveform.

From the timing diagram, we can see that Q2 and Q3 were changing from high to low just before the glitch occurred on RFCK. This means that the counter was transitioning from a count of 15 back to 0. This appears to be the only time the glitch occurs.

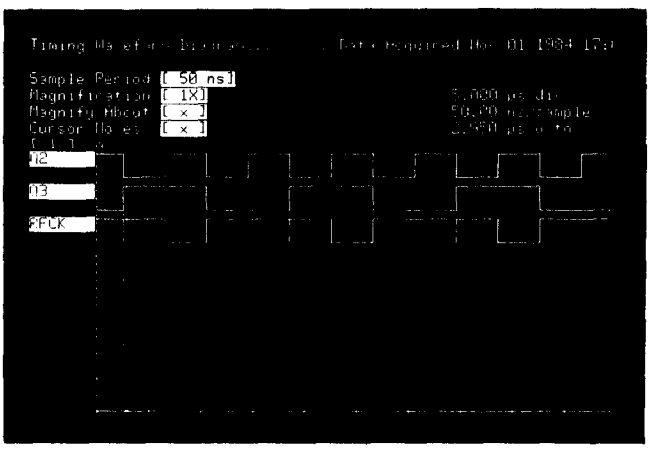


Figure 34

Conclusion: The glitch capture feature of the HP 1631A/D makes it easy to trigger on a glitch. This is especially useful when the glitch occurs intermittently. With the center or end trace mode, you can look at signals before the glitch happened to determine what the cause was. In a later measurement we will use the scope section of the analyzer in conjunction with the glitch capture capability of the timing analyzer to find out in more detail what exactly caused the glitch.

Using The Cross-triggering Capabilities Of The 1631A/D

Introduction To Cross-triggering

This section ties together the previous two sections into what is called cross-analysis triggering. The HP 1631A/D capture data simultaneously with both the analog and timing channels. As we move from the analog realm into timing analysis, we lose some of the raw data. For the most part, that is alright, because we assume that the signals are parametrically correct. If we looked at everything with analog channels, we would be presented with a vast amount of data that in some cases is unneeded. Also, as mentioned before, the timing analyzer has triggering and pattern recognition features that allow us to window on one particular event out of millions. Sometimes, however, the loss of raw data is sorely felt when trying to track down something as elusive as an intermittent glitch. Although, as we saw in the timing analysis section, we can trigger on a glitch with the timing analyzer, it would be extremely useful at times to be able to then look at it with an oscilloscope. Most logic analyzers have a port that can externally trigger an oscilloscope when it finds its trace point. But how do you time-correlate the two displays? In other words, how much time has elapsed from the time the analyzer finds the specified trace point to when the oscilloscope gets the external signal and triggers? If the elusive glitch occurs only once in a while without a recognizable pattern, can we trigger the oscilloscope in time to catch it after the analyzer finds it?

These are the situations where the HP 1631A/D can make a large contribution. Since the scope and logic analyzer capture data simultaneously, what one sees, the other sees. This makes it easy to trace on an event, for instance, with the timing analyzer, and look at that same event with the scope channels, if we suspect a parametric problem. In addition, both the timing and scope channels can he displayed on the same screen at the same time with time correlation. When something happens in the timing display, it happens at the same time in the scope display.

With that in mind, let's move into the third section, "Cross Triggering Capabilities."

Using The Cross-triggering Capabilities Of The HP 1631A/D (continued)

Measurement 9:
Using Cross Triggering To Find The Cause Of A Glitch.

Description: remember the measurement we made in the timing section on capturing a glitch? In the conclusion we indicated that we would find the cause of the glitch with the scope channels. We will use the timing analyzer to capture the glitch, while probing the two inputs to the gate with the scope. This allows us to look at the transitions that cause the glitch in much more detail.

Setup: make the following connections to the DRAM board.

Pod 0 Bit	DRAM Board Connection Point	Signal Name
0	U2 pin 6 (74LS193 pin 6)	Q2
1	U2 pin 7 (74LS193 pin 7)	Q3
2	U9 pin 1 (8409 pin 1)	RFCK

Since we will use the scope and the timing analyzer simultaneously change the system specification to that shown in figure 35.

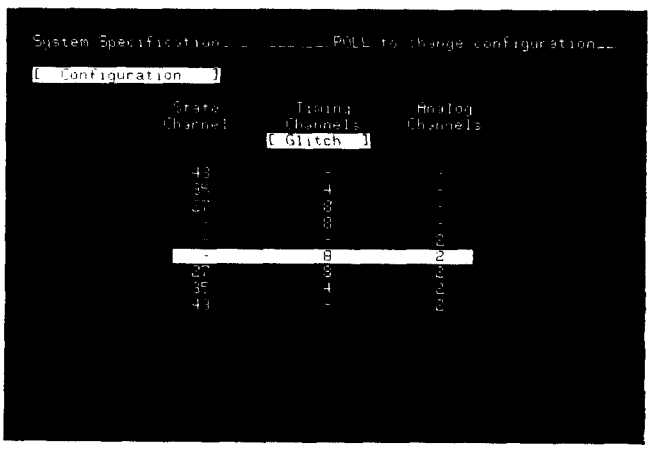


Figure 35

This system specification allows us to use both timing and analog while defining one as the master. This master contains the trace spec, while the slave captures everything (no trace specification).

Set the format specification as shown for timing in figure 36. This specification is the same as for measurement 8.

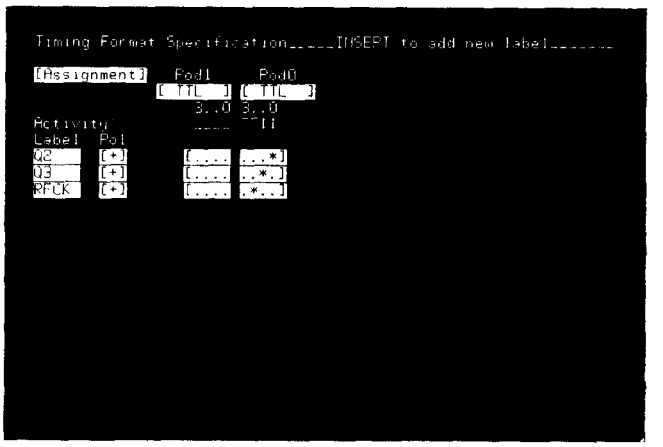


Figure 36

Now set the format specification for the analog channels by pressing the FORMAT key again. Notice that the channel 1 and 2 labels have been changed to Q2 and Q3.

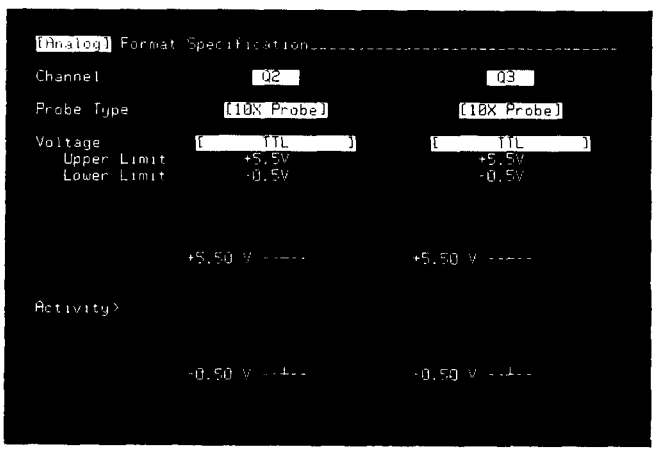


Figure 37

The next task is to set the trace specification. Press the TRACE key and set the trace specification for timing as shown in figure 38. This is the same trace specification we used for measurement 8 except for [Center] trace.

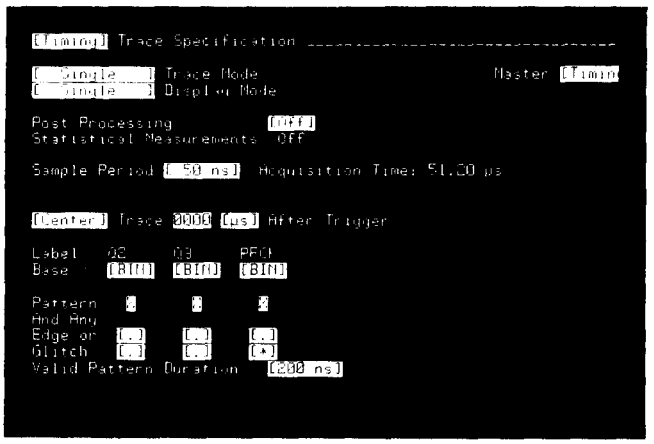


Figure 38

The trace analog specification should be also set for [Center] trace with no other specification. This means that the trigger condition should be set for [Immediate]. You may notice that we have set a different sample period for analog (5 ns) than for timing (50 ns).

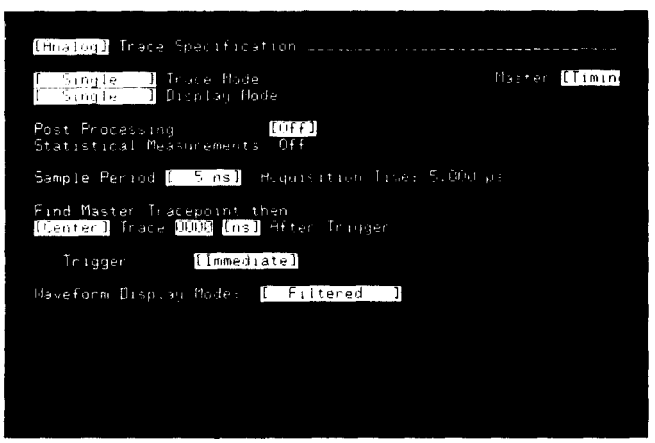


Figure 39

Press RUN on the HP 1631A/D

When the timing diagram is displayed, move the cursor to the channel label for RFCK. Press the INSERT key twice to add two additional channels to the display. Both the new channels will be labelled "Off." Press the PREV[ ] key once. The label field should display Q3, and the waveform will be analog. Move the cursor up to the other "Off' channel, and press the PREV[ ] key twice. Both Q2 and Q3 should be displayed in analog at the bottom of the display. This is the mixed display mode, and should resemble the one shown in figure 40.

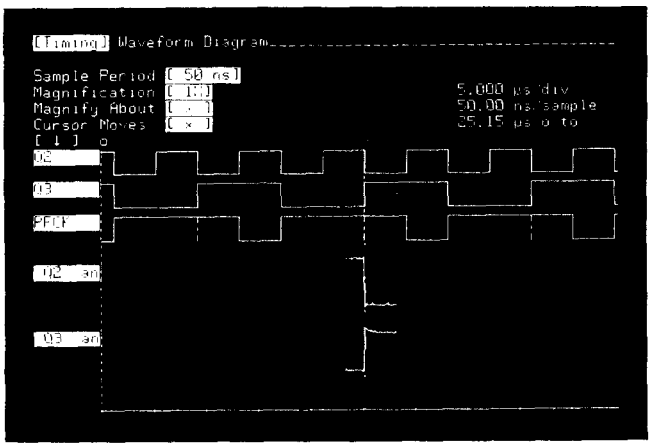


Figure 40

You may have noticed that only a small portion of the analog waveform is displayed around the trace point. This is because the sample period for analog was specified at 5 ns, one-tenth that of timing. Specifying a shorter sample period for analog gives more resolution on the waveform. If you press the WFORM key, the analog waveform is displayed full-screen. Press the WFORM key again to bring the mixed display back on screen.

Move the x and o markers to the tracepoint at center screen, and press the WFORM key to display the analog channels only. Select the [Waveform Diagram] display with the NEXT[ ] key. Change the magnification of the analog display to [40X]. Change the [Time] field to [Volts] and move the o marker on Q2 until a voltage around threshold (1.4 V) is shown as Vo. Move the x marker on Q3 until Vx is also around 1.4 V. In this measurement, we will not worry about hysteresis voltages. Change the [Volts] field back to [Time], and notice that the interval between x and o is around 9 ns. This represents (again without hysteresis) the difference in time of threshold crossings.

When Q2 and Q3 cross TTL threshold, they must do it at the same time or the output of the NAND gate they feed will change. If they do not cross together, the output will change state for a short time (glitch).

For instance, if one input crosses before the other, the output will change to low until both inputs have crossed threshold. As you can see, that is causing the glitch on the RFCK line. Fortunately, the glitch occurs at a non-critical time in the system.

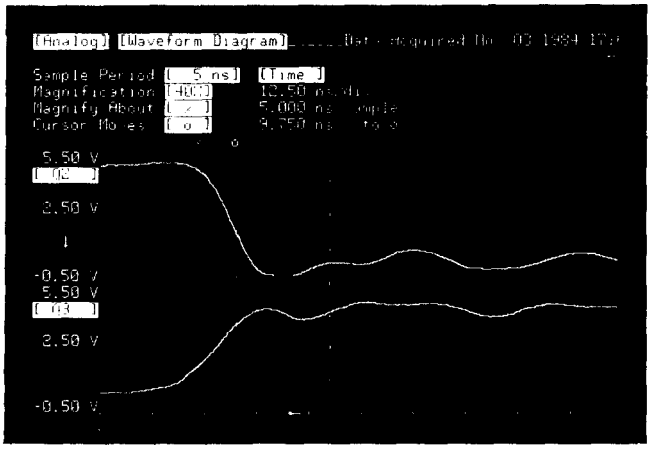


Figure 41

Conclusion: by triggering on a glitch with the timing analyzer and examining in more detail with the analog channels, we could quickly determine the exact cause of the glitch. Had the glitch occurred at a critical time, it would be necessary to load both Q2 and Q3 into a latch and clock them both out at the same time to the NAND gate.

The mixed display mode in the HP 1631A/D allows you to see timing and analog data on one screen, time correlated to one another. In other words, you see on-screen when the events actually happened in time. If more detail on the analog channels is needed, the analog waveforms displayed alone provide that while maintaining time correlation to the timing channels.

The procedure demonstrated here is especially useful when the glitch is intermittent. The timing analyzer with its glitch capture capability can catch the offending transitions, while the analog channels can help determine the cause.

Using The State Analyzer In The HP 1631A/D

Introduction To State Analysis: The Data Domain

As we enter state analysis, we move from the time domain into the data domain. In the time domain, the y-axis of the waveform display is voltage while the x-axis is time. In the data domain, we are not concerned about time except in the sense that one thing happens before another. State analysis is a functional test that monitors one state after another of the microprocessor.

The fundamental difference between timing/parametric analyzers and state analyzers is the method of sampling. The timing analyzer and digital oscilloscope depend on a high sample rate that is asynchronous to the system under test. 'This high sample rate allows the analyzer to get a representation of what is happening. If the sample rate is too slow, there is the danger of Nyquist aliasing. The state analyzer, on the other hand, runs syncronously with the system and captures discrete steps. Each of these steps occurs in sync with the system clock, and there are no events of interest between these steps.

A total explanation of logic state analyzers is beyond the scope of this guide. If you arc unfamiliar with state analysis and the necessary features of a state analyzer, consult other books on the subject. For a primer, Logic Analyzers For Microprocessors by John Kneen is a good starting point. It is published by the Hayden Publishing (Company.

Using The State Analyzer In The HP 1631A/D (continued)

Measurement 10:
Using The State Analyzer To Capture A Simple Program

Description: In this first measurement of the state section we will enter a simple program into the 5036A microprocessor lab and capture it with the state analyzer.

Setup: push the SYSTEM key at the top left of the keyboard and roll the configuration bar to the top as shown in figure 42. This configures the analyzer for 43 state channels.

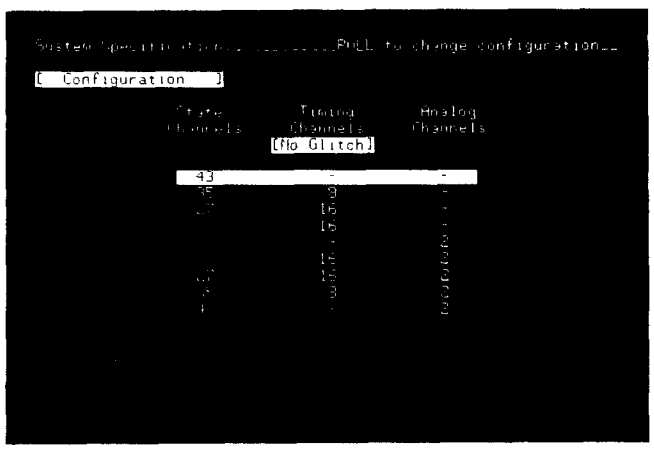


Figure 42

Plug the probes into the HP 10269B as follows:

102698 socket	1631 pod number
-	0
A	1
C	2
D	3
B	4

Connect the HP 64655A preprocessor module into the bottom of the HP 10269B. Remove the 8085 from the 5036A (make sure the power to the 5036A is off), and plug the cable from the HP 64655A into the processor socket. Plug the 8085 into the socket from the HP 64655A. Power the 5036A up. All of the physical connections to the 8085 are now made without the need to clip on individual leads.

Connect an HP 9121S/D or HP 9122S/D to the HP 1631A/D via the HP-IB cable. Place the 10304B disk into the disc drive and power it up. Press the SYSTEM key on the HP 1631A/D and use the NEXT[ ] key to bring up the disk operations menu. This menu will show the directory of the disk after you press the INSERT key on the 1631. Using rhe ROLL keys, select the 8085 inverse assembler. Using the field at the bottom of the screen and the NEXT[ ] key, set the analyzer to [Load] file type [invasm] named 18085. Press the INSERT key on the 1631 to start the operation. The inverse assembler configures the analyzer for use with the 8085 and relieves you of the need to assign all of the pod bits. It also labels all of the appropriate user base fields for status. Lastly, it interprets bit patterns on the data bus and allows you to display them as assembly instructions instead of hexadecimal codes.

Follow the sequence listed to enter a short program into the 5036A. This is the program we will capture with the state analyzer.

FETCH ADDR 8000	Fetch address 8000
c3	jump to address 8050
STORE/INCR 50	
STORE/INCR 80	
STORE/INCR FETCH ADDR 8050	. Jump to address 9000
C3 STORE/INCR 00 90	
FETCH ADDR 9050	
C3 STORE/ INCR 00	Jump to address 8000
STORE/INCR 80	
STORE/INCR FETCH ADDR 8000	Fetch address 8000
RUN	Run the program

This simple program starts at address 8000. Stored in address 8000 is the instruction to jump (C3). The next two locations (8001 and 8002) contain the address to jump to 8050. Address 8050 contains another jump command and the next two bytes also tell the processor where to jump to 9000. As you might guess, address 9000 contains a third jump command, and addresses 9001 and 9002 give a jump-to address of 8000, which is the start of the program. The program thus starts at address 8000, jumps to 8050, jumps to 9000, and then back to 8000 to start all over again. It continues until stopped.

Press the TRACE key on the HP 1631A/D and set it as shown in figure 43.

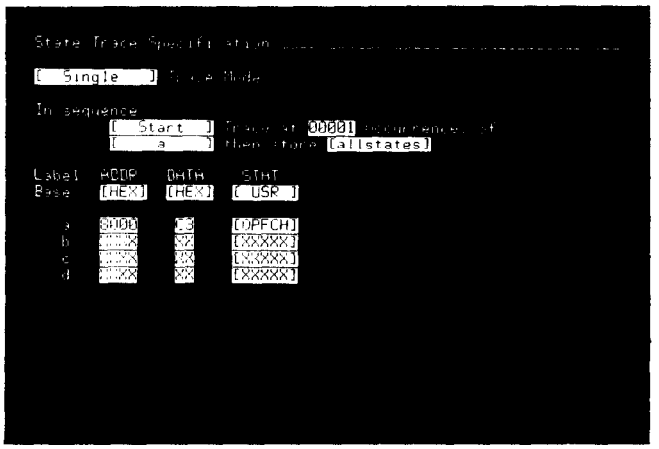


Figure 43

Press the RUN key on the HP 1631A/D and look at the resulting state listing. Notice that in the listing the analyzer captured address 8000 that contained data C3, which is a JUMP command. Immediately following are addresses 8001 and 8002, which contain the the number 8050 in two bytes, least significant first (which is the way most, if not all, 8-bit processors send data on the data bus). After address 8002 is 8050 with another JUMP command (C3) in data, followed by two bytes of address for the jump, in this case 9000. As you may have noticed, the display lists the complete program and-then starts over, as might be expected since the program continues in a loop. Using the ROLL keys you can examine as much of the list as you like.

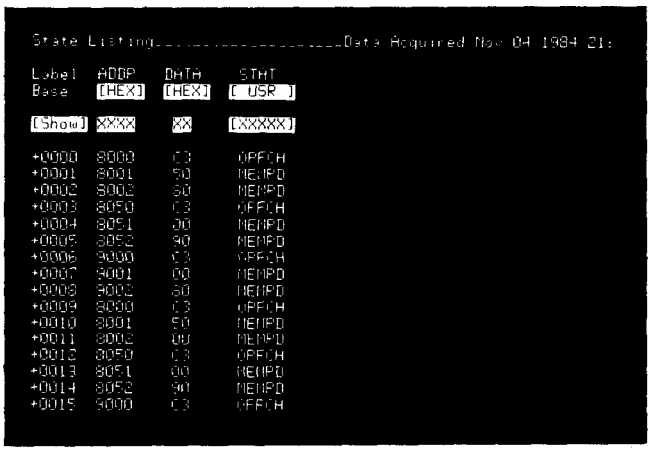


Figure 44

Move the cursor to the bracketed field below the DATA heading and press the NEXT[ ] or PREV[ ] key until the data listing changes to inverse assembly. This is one of the functions of the inverse assembler you loaded from disk at the start of the setup. As you can see, the inverse assembled listing makes it much easier to keep track of what is going on than a lot of hexadecimal codes representing what the processor sees.

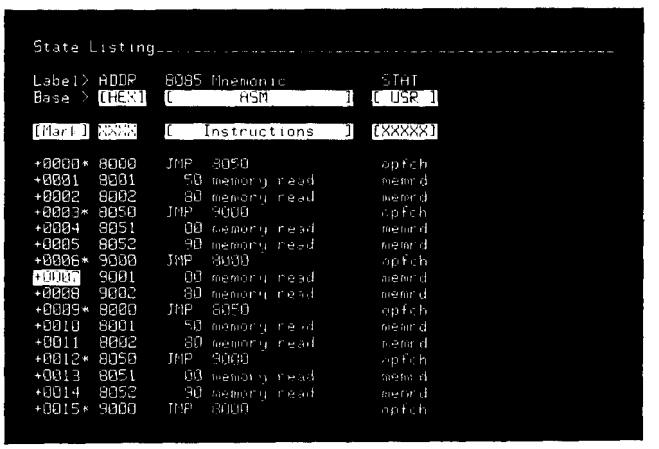


Figure 45

Change the trace specification to match the one shown in figure 45. This tells the analyzer to find the first occurrence of a (i.e., address 8000, with data C3); instead of storing all states, it selectively stores only jump commands. Press the RUN key on the HP 1631A/D and look at the resulting state listing. Only those addresses that contain data C3 (JUMP) are stored and listed. This is one of the capabilities of the state analyzer to capture and store specified events.

Appendix A:
Overview Of DRAMs And The DRAM Board For The 5036A

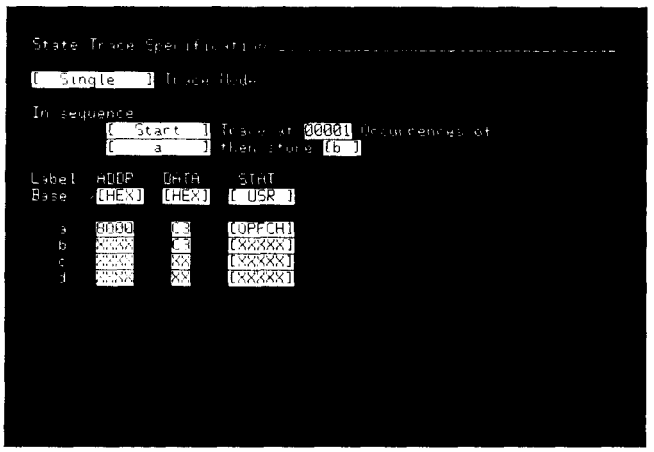


Figure 46

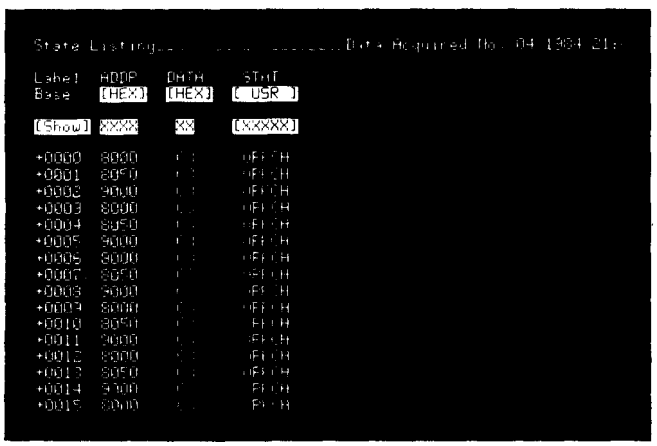


Figure 47

Conclusion: a state analyzer is the appropriate tool for capturing processor activity, just as an oscilloscope is an appropriate tool for capturing waveforms. Here we entered a short, simple program, and then proceeded to capture and examine it with the state analyzer. While there are many more capabilities in the state analyzer that we will not explore, you now have enough knowledge to use the state analyzer for simple state analysis.

A Brief Introduction To DRAMs

Addressing

The DRAMs used in the demonstration board have a physical architecture of 128 rows by 512 columns. To address a particular bit in the RAM, the memory needs a row address and column address, similar to Cartesian coordinates. Each row has 512 bits across, which relate to the column address. The eight address pins on the RAM are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of a memory cycle by two clocks (active negative called the row address strobe (RAS) and a column address strobe (GAS)). A total of sixteen address bits decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by specified minimum and maximum times.

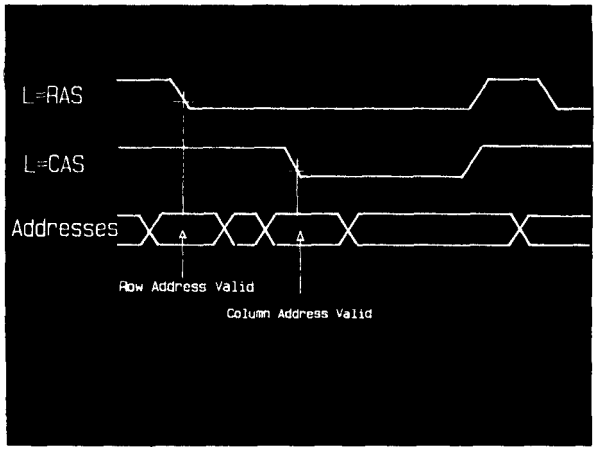


Figure 48

Memory Read/Write Cycles

The memory read cycle begins with the row addresses valid and the RAS clock transitioning from high to low. The CAS clock must also make a transition from high to low within a specified time limit when the column addresses are latched. After the clocks have become active, they must stay active for the minimum period specified by the manufacturer.

Data out is not latched and is valid as long as the CAS clock is active; the output will switch to the three-state mode when the CAS clock goes inactive. The CAS clock can remain active for a maximum of 10 ns into the next cycle. To perform a read cycle, the write enable (WE) input must be held high from the time the CAS clock makes its active transition (high to low) to the time when it transitions into the inactive mode.

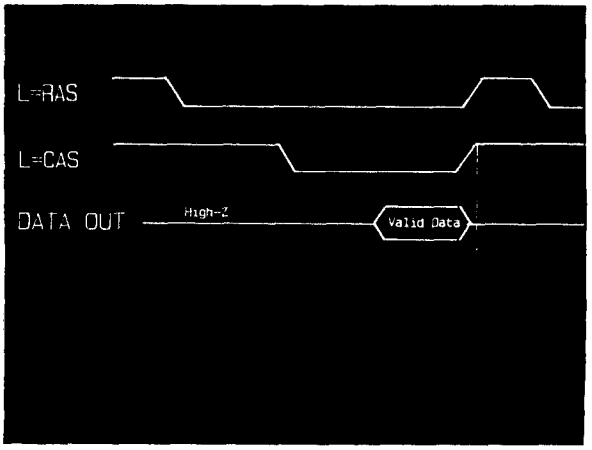


Figure 49

A write cycle is similar to a read cycle except that the WE clock must become active at or before the CAS clock becomes active.

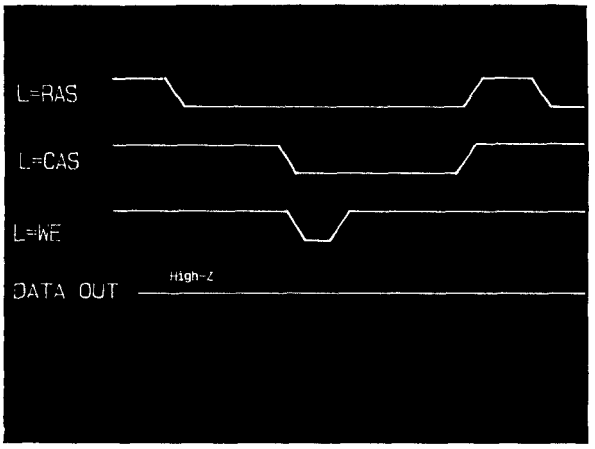


Figure SO

Appendix A: Overview Of DRAMs And The DRAM Board (continued)

Refresh Cycles

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge tends to degrade with time and temperature. Therefore, to retain the correct information, the bits must be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms or at least one row every 15.6 μs. A normal read or write operation to the RAM refreshes all the bits (256) associated with that particular row decoded. In other words, whenever a RAS pulse is applied to a particular row, all cells in that row are refreshed.

Two basic modes of refreshing are used in our DRAM board--hidden and forced. The 8409 chip controller generates most of the timing signals needed by the RAMs and also keeps track of when they must be refreshed.

Hidden Refresh

A chip select line on the 8409 enables it to know when the system is accessing the RAMs or something other than the RAMs. The 8409 maintains an on-board counter that i-r cycles through to be able to address all 128 rows of the RAMs within the 2ms maximum refresh cycle time. It stays with each row 16 μs (2 ms/128 rows), as determined by RFCK (REFRESH CLOCK). During the high portion of RFCK, if the 8409 sees via the chip select line that the processor is busy elsewhere, it slips in a refresh to the current row on all the DRAMs. This is called a hidden refresh, since the system processor never knows that the RAMs have been refreshed.

Forced Refresh

If during a 16 μs refresh cycle the processor does not turn loose of the chip select line so the DRAM controller can perform a hidden refresh, the controller performs what is called a forced refresh. When RFCK transitions from high to low, the 8409 checks an internal flip-flop that indicates whether a hidden refresh has occurred within that cycle. If not, it pulls a line high that is inverted and applied to the processor HOLD line. This requests that the processor finish the current instruction cycle and grant the 8409 control of the address bus. When the bus is granted to the DRAM controller, the controller refreshes the current row of DRAMs. The disadvantage of a forced refresh is that rhe processor is idle during the time that the RAMs are being refreshed.

National Semiconductor

November 1982

DP8409 Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. the DP8409 Multi-Mode Dynamic RAM Controller/Driver. The DP8409 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500pF loads with propagation delays of 25ns. The DP8409 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409 has 3 mode-control pins: M2, MI, and MO, where M2 is in general REFRESH. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{RAS}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{RAS}$ outputs are selected, while CAS is inhibited.

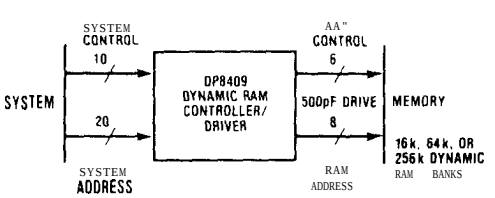
The DP8409 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs RAS, CAS, and $\overline{WE}$ are provided with the same drive capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while CAS, WE, and the multiplexed addresses can be connected lo all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE". Only the bank with its associated $\overline{RAS}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k, 64k, and 256k DRAMs
- Capable of addressing 64k, 256k, or 1M words
- Propagation delays of 25ns typical at 500pF load
- $\overline{CAS}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{RAS}$, row to column select, then $\overline{CAS}$ automatically and fast
- $\overline{WE}$ follows $\overline{WIN}$ unconditionally-offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255, or 511)
- End-of-Count indicated by RF I/O pin going low at 127, 255, or 511
- Low input on RF I/O resets 9-bit refresh counter
- $\overline{CAS}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE. and End-of-Count set to 127

Mode Features

- 8 modes of operation: 3 access, 3 refresh, and 2 set-up
- 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{RAS}$ → R/$\overline{C}$ → CAS automatic, with t_{RAH} = 20 or 30ns minimum (Modes 5, 6)
- Auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after system acknowledge of request (Mode 1)
- Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)
- 2 All-$\overline{RAS}$ Access modes externally or automatically controlled for memory initialization (Modes 3a, 3b)
- Automatic All-RAS mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End-of-Count value of Refresh Counter set by B1 and BO (Mode 7)



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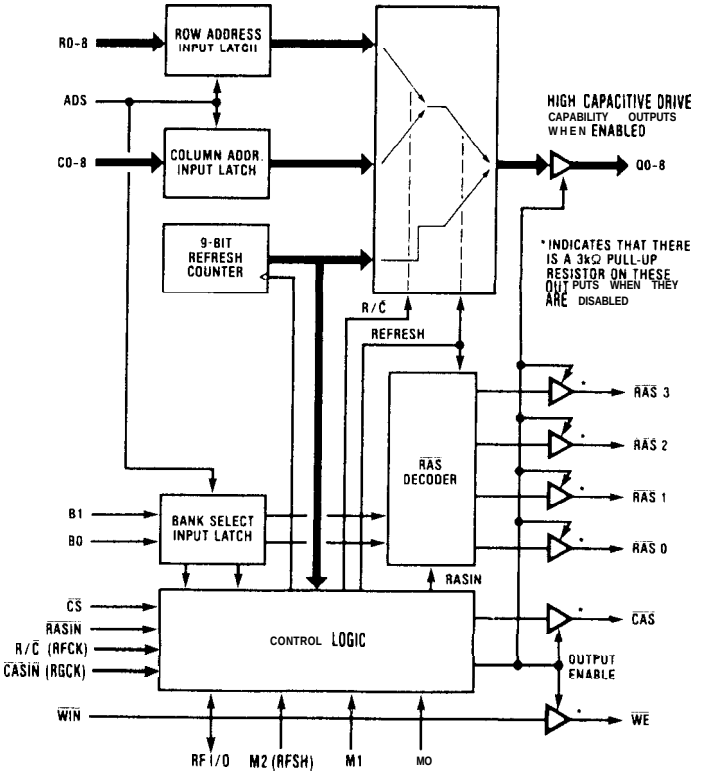
Appendix A:
Overview Of DRAMs And The DRAM Board (continued)



DP8409 Functional Block Diagram

Table 1. DP8409 Mode Select Options

Mode	($\overline{RFSH}$) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto Refresh — forced	RF I/O = Refresh Request ($\overline{RFRQ}$)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = $\overline{EOC}$
3a	0	1	1	All $\overline{RAS}$ Auto Write	RF I/O = $\overline{EOC}$; All $\overline{RAS}$ Active
3b	0	1	1	Externally Controlled All $\overline{RAS}$ Access	All $\overline{RAS}$ Active
4	1	0	0	Externally Controlled Access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto Access, Fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set End of Count	See Table 3 for Mode 7

Pin Definitions

V_{CC}, GND, GND — V_{CC} = 5V ± 5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

RO- R8: Row Address Inputs.

C0-C8: Column Address Inputs.

Q0-Q8: Multiplexed Address Outputs — Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

RASIN: Row Address Strobe Input — Enables selected RAS, output when M2 (RFSH) is high, or all $\overline{RAS}_n$ outputs when RFSH is low.

R/C (RFCK) — In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input: selects either the row or column address input latch onto the output bus.

CASIN (RGCK) — In Auto-Refresh Mode, Auto Burst Mode, and All-RAS Auto-Write Mode, this pin is the RAS Generalor Clock input. In all other modes it is CASIN (Column Address Strobe Input), which inhibits CAS output when high in Modes 4 and 3b. In Mode 6 it can be used to prolong CAS output.

ADS: Address (Latch) Strobe Input — Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; Latches on high-to-low transition.

CS: Chip Select Input — TRI-STATE's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

MO, M1, M2: Mode Control Inputs — These 3 control pins determine the 6 major modes of operation of the DP8409 as depicted in Table 1.

RF I/O — The I/O pin functions as a Reset Counter Input when set low from an external opencollector gate, or as a flag output. The flag goes active-low in Modes 0 and 2 when the End-of-Count output is at 127, 255, or 511 (see Table 3). in Auto-Refresh Mode it is the Refresh Request output.

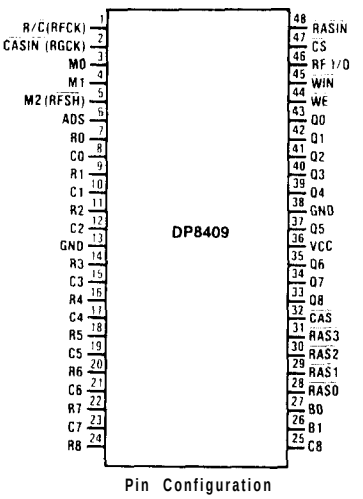
WIN: Write Enable Input

WE: Write Enable Output — Buffered output from WIN.

CAS: Column Address Strobe Output — In Modes 3a, 5, and 6, CAS transitions low following valid column address. In Modes 3b and 4. it goes low after R/C goes low, or follows CASIN going low if R/C is already low. CAS is high during refresh.

RAS O-3: Row Address Strobe Outputs — Selects a memory bank decoded from B1 and B0 (see Table 2), if RFSH is high. If RFSH is low, all banks are selected,

B0, B1: Bank Select Inputs — Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes low. Also used to define End-of-Count in Mode 7 (Table 3).



Pin Configuration

Conditions for all Modes

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, RASIN and R/C are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (BO and B1). If CS is low, all outputs are enabled. When CS is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If CS is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The DP8409 has timing parameters that are specified with up to 600 pF loads. In a typical memory system this is equivalent to about 68, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 10. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

DP8409 Driving any 16k or 64k DRAMs

The DP8409 can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are Interchangeable (for the same supply-rail chips), and the DP8409 can drive all 16k DRAMs (see Figure la).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8409 can drive all three configurations, and at the same time allows them all to be Interchangeable (as shown in Figures lb and lc), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2ms (i.e. 256 rows in 4ms) all DRAM types are correctly refreshed.

When the DP8409 is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 512 to accommodate 16k, 64k, or 256k DRAMs. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 before roiling over to zero.

DP8409 Interlace Between System & DRAM Banks

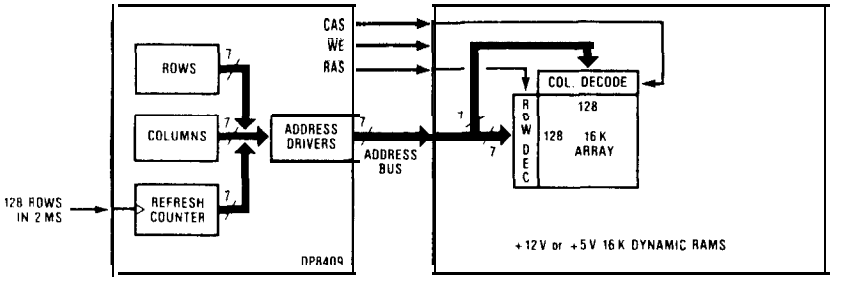


FIGURE la. **DP8409 with any 16k DRAMS**

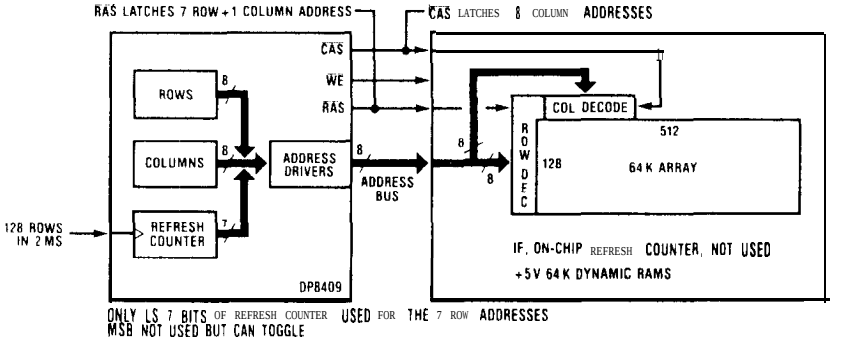


FIGURE lb. DP8409 with 128 Row x 512 Column 64k DRAM

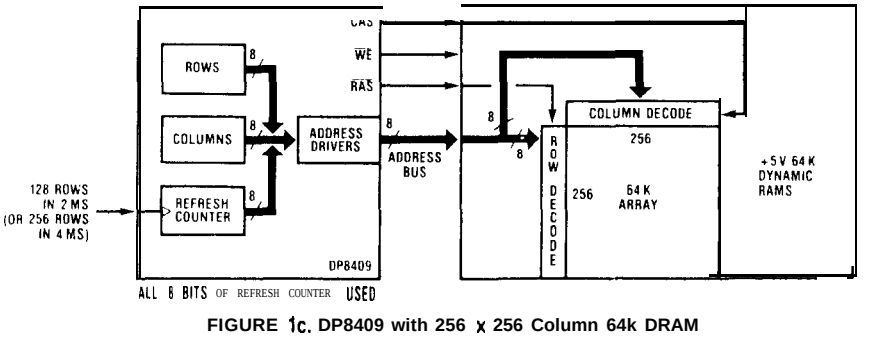


FIGURE 1c. DP8409 with 256 x 256 Column 64k DRAM

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as CAS goes low If $\overline{WE}$ goes low later than t_{CWD} after CAS goes low. first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address IN the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When Vcc IS first applied to the DP8409, an initialize pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} Increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As Vcc Increases above 2.3 volts, control of these outputs is granted to the system.

DP8409 Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8409. Substitute the respective delay numbers for the DP8409-2 or DP8409-3 when using these devices.

Mode 0 — Externally Controlled Refresh

Figure 2 is the Externally Controlled Refresh Timing. In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following RASIN, and $\overline{CAS}$ is Inhibited. This refreshes the same row in all four banks. The refresh counter increments when either RASIN or RFSH goes low-to-high while the other is low. RF I/O goes low when the count is 127.255, or 511, as set by End-of-Count (see Table 3), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $\overline{RFSH}$ can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after RFSH goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before RAS occurs on all RAS outputs, strobing the counter address into that row of all the DRAMs. Refer to Figure 2. To perform externally controlled burst refresh, RFSH initially can again have the same edge as RASIN, but then can maintain a low state, since RASIN going low-to-hrgh increments the counter (performing the burst refresh).

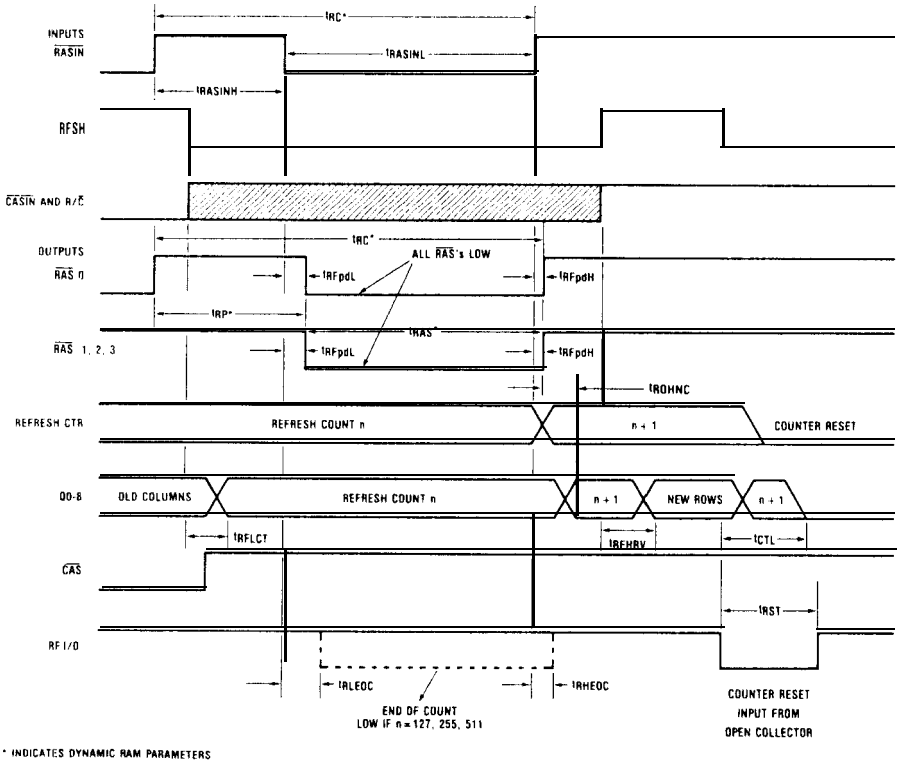


FIGURE 2. External Control Refresh Cycle (Mode 0)

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

Mode 1 — Automatic Forced Refresh

In Mode 1, the R/C (RFCK) pin becomes RFCK (refresh cycle clock), instead of R/C, and CAS remains high. If RFCK is kept permanently high, then whenever M2 (RFSH) goes low, an externally controlled refresh will occur and all RAS outputs will follow RASIN, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but when set low externally through an open-collector driver, the refresh counter resets as normal. This externally controlled method may be preferred when operating in the Automatic Access mode (Mode 5), where hidden or forced refreshing is undesirable, but refreshing is still necessary.

If RFCK IS an input clock signal, one (and only one) refresh cycle must take place every RFCK cycle. Refer to Figure 9. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O (Refresh Request) goes low Immediately after RFCK goes low, indicating to the system that a forced refresh is requested. The system must allow a forced refresh to take place while RFCK is low (refer to Figure 3). The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 (RFSH) pin, a forced-refresh cycle will be initiated by the DP8409, and RAS will be internally generated on all four RAS outputs, to strobe the refresh counter contents on the address outputs into all the DRAMs. An external RAS Generator Clock (RGCK) is required for this function. It is fed to the CASIN (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), RAS remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; RAS then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to RAS going low, M2 should go low t_{RFSRG} before the next failing edge of RGCK. The Refresh Request on RF I/O is terminated as RAS begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh RAS will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh RAS end in less than 2 periods of RGCK from the time RAS went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and RAS will go high t_{RFRH} after M2.

To allow the forced refresh, the system will have been inactive for about 4 periods of RGCK, which can be as fast as 400ns every RFCK cycle. To guarantee a refresh of 126 rows every 2 ms, a period of up to 16 µs is required for RFCK. In other words, the system may be down for as little as 400ns every 16 µs, or 2.5% of the time. Although this is not excessive, it may be preferable to perform a Hidden Refresh each RFCK cycle, which is allowed while still in the Auto-Access mode, (Mode 5).

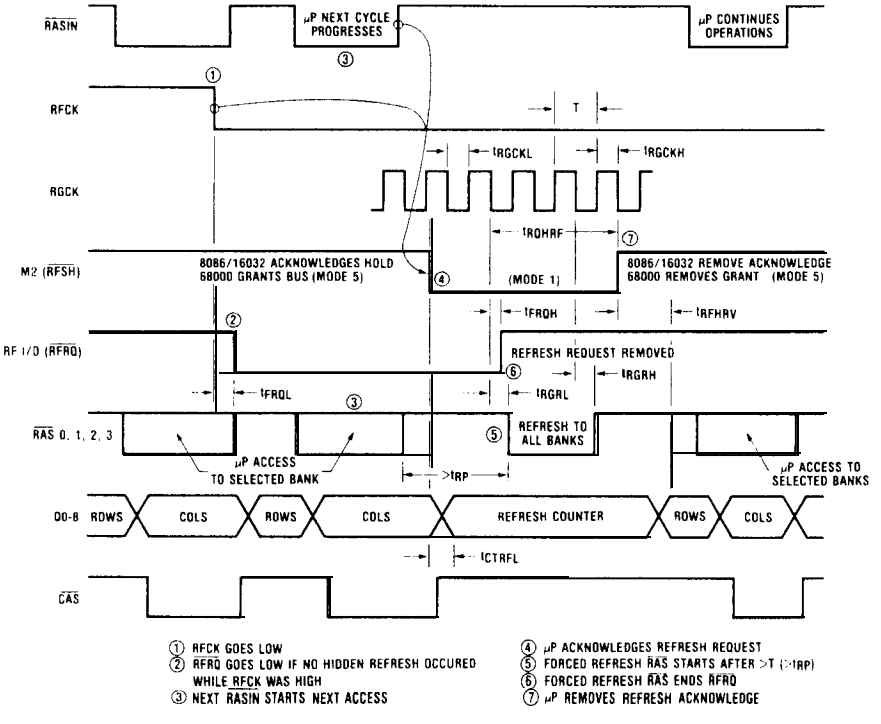


FIGURE 3. DP8409 Performing a Forced Refresh (Mode 5-I-S) with Various Microprocessors

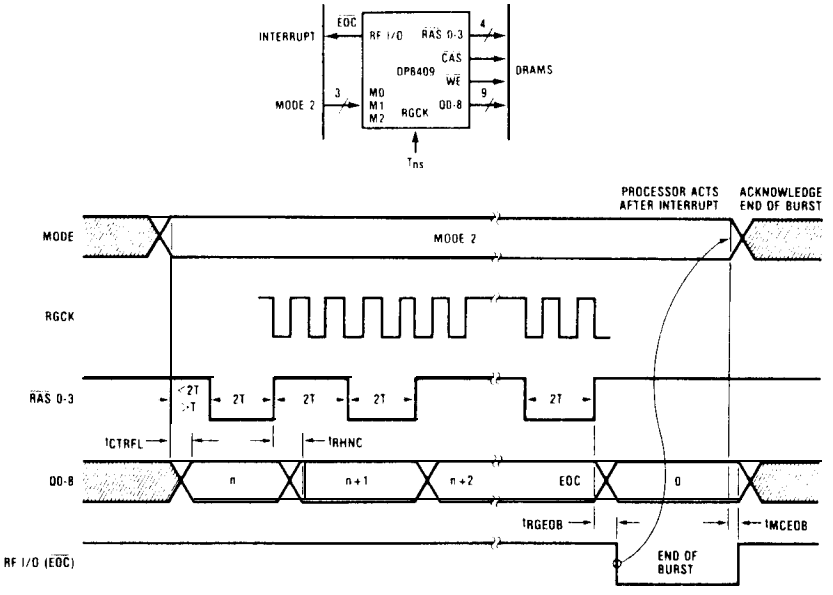


FIGURE 4. Auto-Burst Mode, Mode 2

Mode 2 — Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 4). When the DP8409 enters this mode, CASIN (RGCK) becomes the RAS Generator Clock (RGCK), and RASIN is disabled. CAS remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last RAS has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to Indicate the End-of-Burst condition.

The signal on all four RAS outputs is just a divide-by-four of RGCK. In other words, if RGCK has a 100 ns period, RAS is high and low for 200ns each cycle. The refresh counter increments at the end of each RAS, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100 ns period with End-of Count set to 127. RF I/O will go low after 126 x 0.4 µs, or 51.2 µs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the DPH409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after 26 µs), power can then be removed from the DP6409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the DP6409.

Mode 3a — All-RAS Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All RAS outputs are activated, as in refresh, and so are CAS and WE. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations.

To select this mode, B1 and BO must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16k DRAMs, B1 and B0 are 00. For 64k DRAMs, B1 and BO are 01, so that for the configuration of Figure lb, the 6 refresh counter bits are strobed by RAS into the 7 row addresses and the ninth column address. After this Automatic-Write process, B1 and B0 must be set again in Mode 7 to 00 to set End-of-Count to 127. For the configuration of Figure lc, B1 and B0 set to 01 will work for Automatic-Write and End-of-Count equals 255.

In this mode, R/C is disabled, WE is permanently enabled low, and CASIN (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127,255, or 511 (as set by End-of-Count in Mode 7). and the RAS outputs are active.

Referring to Figure 5a, an external 8-bit counter (for 64k DRAMs) with TRI-STATE outputs is required and must be connected to the column address Inputs. It is enabled only during this mode, and is clocked from RF I/O The DP6409 refresh counter is used to address the rows, and the column address is supplied by the external counter. Every row for each column address is written to in all four banks. At the End-of-Count RF I/O goes low, which clocks the external counter.

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

Therefore, for each column address, the refresh counter first outputs row-0 to the address bus and all four $\overline{RAS}$ outputs strobe this row address into the DRAMs (see Figure 5b). A minimum of 30ns after $\overline{RAS}$ goes low (t_{RAH} = 30 ns), the refresh counter is disabled **and the** column address input latch is enabled onto the address bus About 14ns after the column address is valid, $\overline{CAS}$ goes low, (t_{ASC} = +14 ns), strobing the column address into the DRAMs. When $\overline{RAS}$ and $\overline{CAS}$ go high the refresh counter Increments to the next row and the cycle repeats. Since $\overline{WE}$ is kept low In this mode, the data at DI (input data) of the DRAMs is written into each row of the latched column. During each cycle $\overline{RAS}$ is high for two periods of RGCK and low for two periods, giving a total write-cycle time of 400ns minimum, which IS adequate for most 16k and 64k DRAMs. On the last row of a column, RF I/O increments the external counter to the next column address

At the end of the last column address, an interrupt is generated from the external counter to let the system know that initialization has been completed. During the entire initialization time, the system can be performing other initialization functions This approach to memory initialization is both automatic and fast. For instance, if four banks of 64k DRAMs are used, and RGCK is 100 ns, a write cycle to the same location in all four banks takes 400 ns, so the total time taken in initializing the 64k DRAMs is 65k X 400 ns or 26 ms. When the system receives the interrupt, the external counter must be permanently disabled. ADS and $\overline{CS}$ are interfaced by the system, and the DP8409 mode is changed. The interrupt must then be disabled.

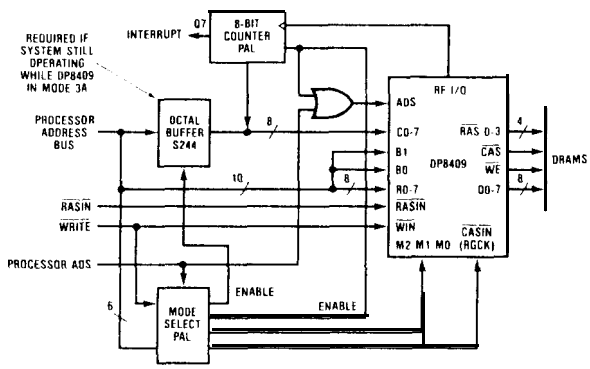


FIGURE 5a. DP8409 Extra **Circuitry Required for All-RAS Auto Write Mode, Mode 3a**

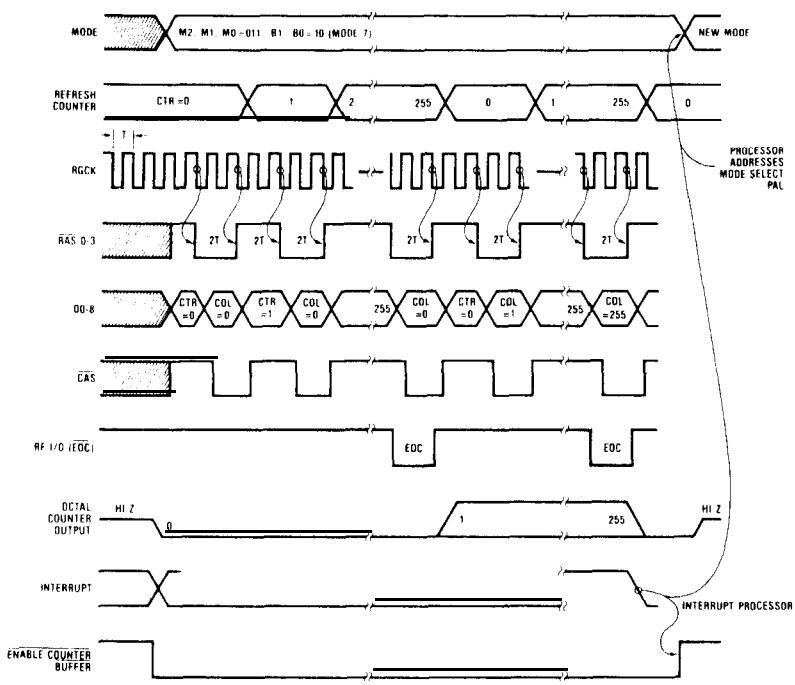


FIGURE 5b. DP8409 All-RAS Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b — Externally Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow RASIN (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while CASIN may be used to control CAS (as in the Externally Controlled Access mode), so that CAS strobes the column address contents into the DRAMs. At this time WE should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8409 for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However. initialization sequence timing is under system control. which may provide some system advantage.

Mode 4 — Externally Controlled Access

This mode facilitates externally controlling all access. timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 6.

Output Address Selection

Refer to Figure 7a. With M2 (RFSH) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output QO-08, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. RASIN can go low after the row address. es have been set up on 00-08. This selects one of the RAS outputs, strobing the row address on the 0 outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go tow so that about 40 ns later column addresses appear on the 0 outputs.

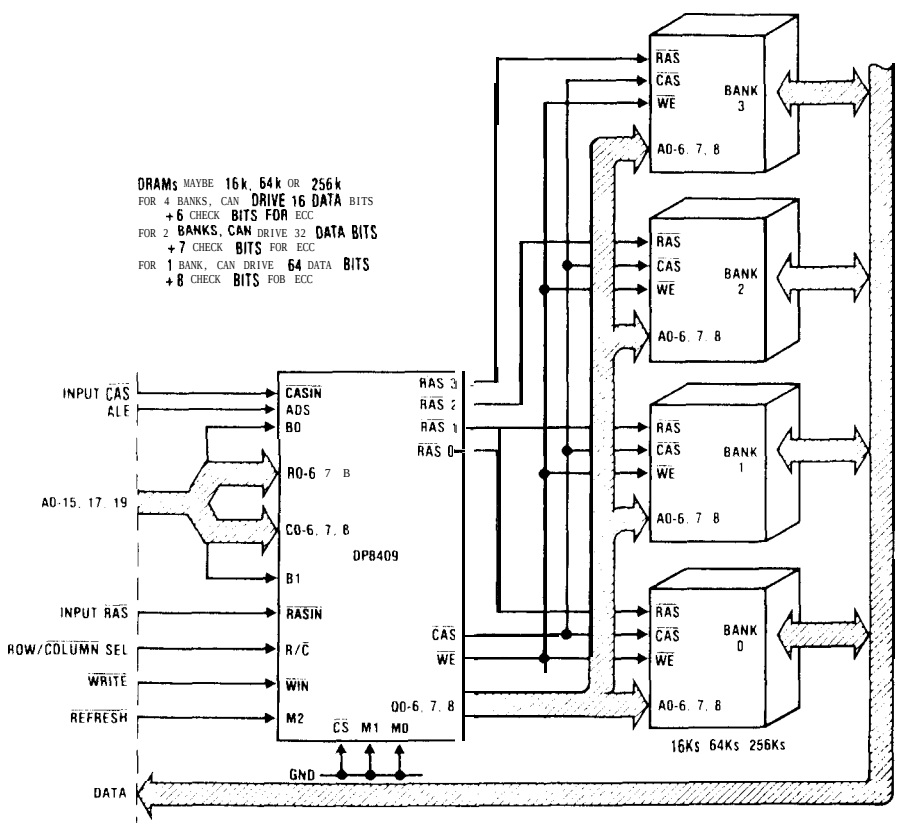


FIGURE 6. Typical Application of DP8409 Using External Control Access and Refresh In Modes 0 and 4

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

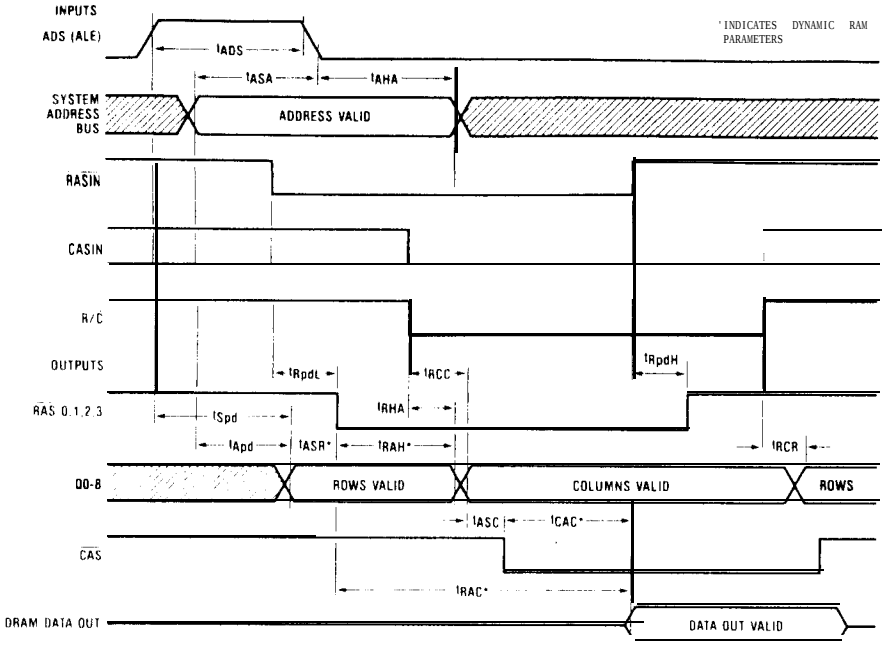


FIGURE 7a. Reed Cycle Timing (MODE 4)

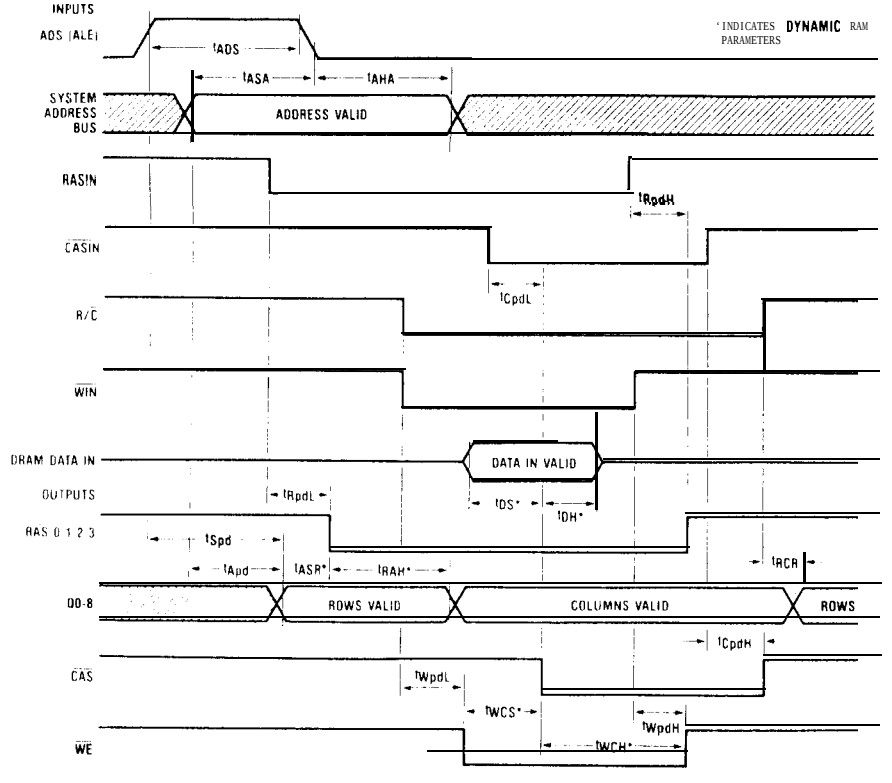


FIGURE 7b. Write Cycle Timing (Mode 4)

Automatic CAS Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs CASIN or R/$\overline{C}$. If CASIN is high, then R/$\overline{C}$ going low switches the address output drivers from rows lo columns. CASIN then going low causes $\overline{CAS}$ to go low approximately 40ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 7b). For maximum system speed, CASIN can be kept low, since $\overline{CAS}$ will automatically occur approximately 20ns after the column addresses are valid, or about 60ns after R/$\overline{C}$ goes low (see Figure 7a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of Ons or −10ns. In other words, a t_{ASC} greater than Ons is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay ($t_{RPDL} + t_{RAH} - t_{RHA}$) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

Mode 5 — Automatic Access with Hidden Refresh

The Auto Access with Hidden Refresh mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and CASIN are unnecessary and can be used for other functions (see Refreshing, below). Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 land Mode 6) of the DP8409 make DRAM accessing appear essentially "static".

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8409 in this mode.

Provided the input address is valid as ADS goes low, RASIN can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27ns later, by which time the row address is already valid on the address output of the DP8409. The Address Set-Up time (t_{ASR}), is Ons on most DRAMs. The DP8409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of Ons. This is true provided the input address was valid t_{ASA} before ADS went low (see figure 8a).

Next, the row address is disabled after t_{RAH} (30ns minimum), in most DRAMs, t_{RAH} minimum is less than 30ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is WIN. When a write cycle is required, WIN must go low at least 30ns before $\overline{CAS}$ is output low.

This gives a total typical delay from. input address valid to RASIN (15ns); to $\overline{RAS}$ (27ns); to rows held (50ns); to columns valid (25ns); to $\overline{CAS}$ (23ns) = 140ns (that is, 125ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is RASIN.

Refreshing

Because R/$\overline{C}$ and CASIN are not used in this mode, R/$\overline{C}$ becomes RFCK (refresh clock) and CASIN becomes RGCK ($\overline{RAS}$ generator clock). With these two signals it is possible to perform refreshing without extra ICs, and without holding up the processor.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2ms (one row every 16μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16μs. RFCK going high sets an internal refresh-request flip-flop. First the DP8409 will attempt to perform a hidden refresh so that the system throughput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the DP8409 goes high and RASIN occurs, a hidden refresh will occur. In this case, RASIN should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the DP8409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow RASIN. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK. Refer to Figure 9.

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400ns and RFCK is high for 8μs, then the system has 20 chances lo not select the **DP8409.** If during this time a hidden refresh did not occur, then the DP8409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After AFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 (RFSH) low does the DP8409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 3. The internal refresh request flip-flop is then reset.

Figure 9 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go TRI-STATE until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50-percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the DP8409's forced-refresh request.

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

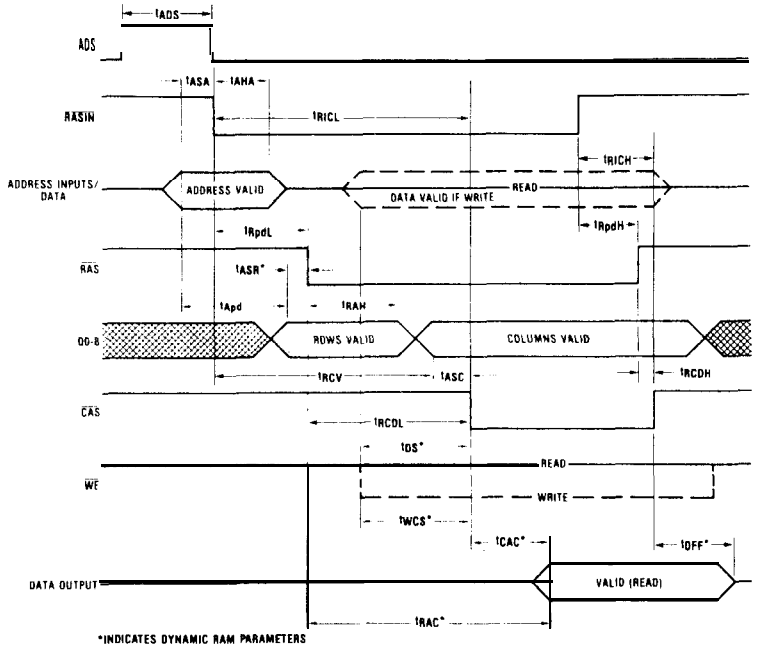


FIGURE 8a. Modes 5, 6 Timing ($\overline{\text{CASIN}}$ High in Mode 6)

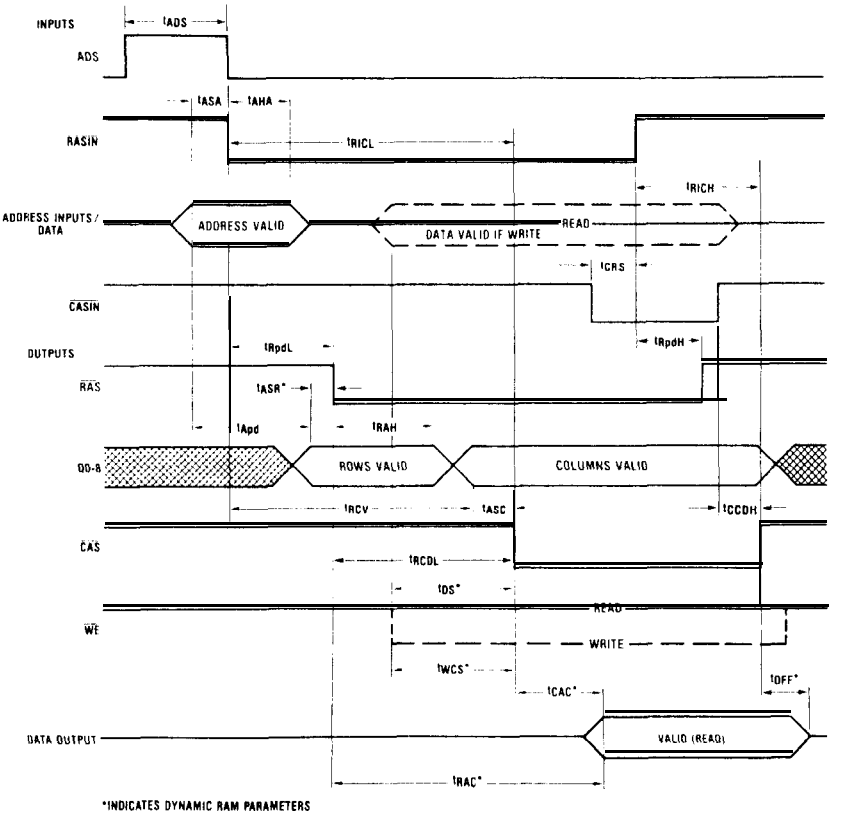


FIGURE 8b. Mode 6 Timing, Extended CAS

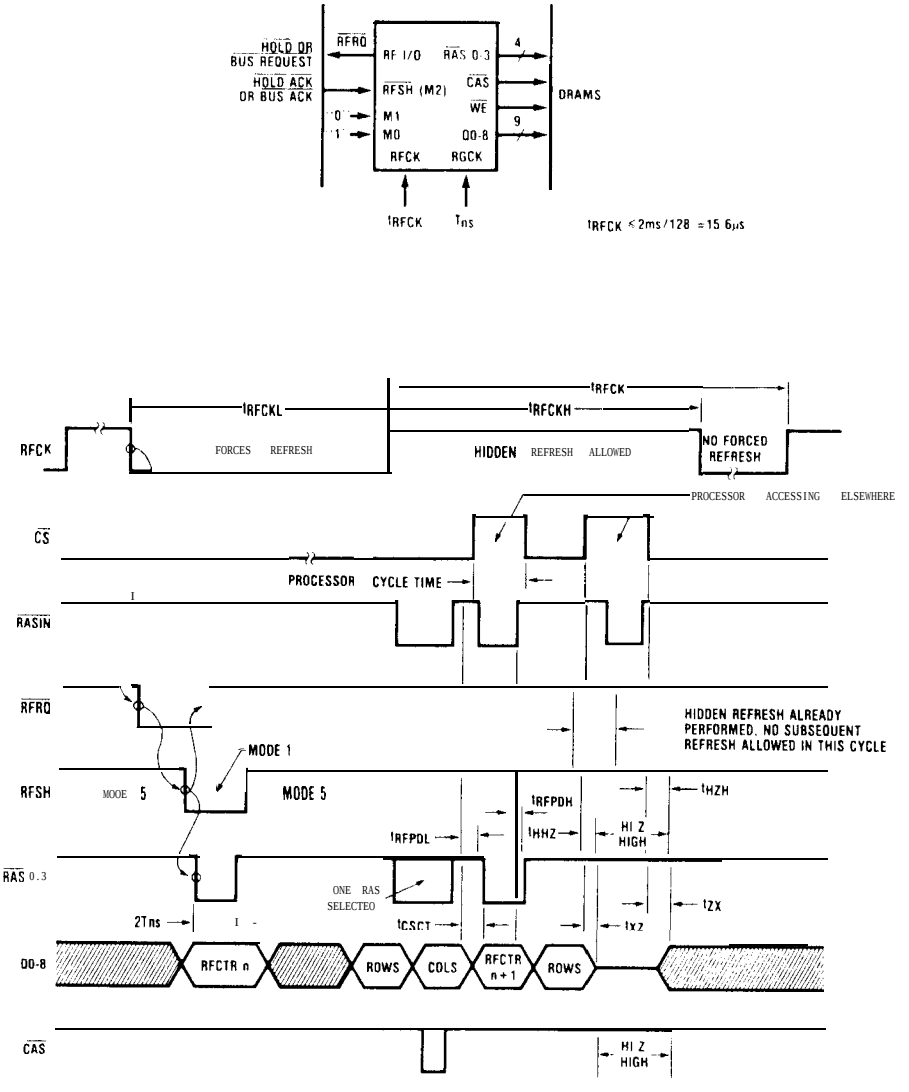


FIGURE 9. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

Table 2. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Note that RASIN going low earlier than t_{CSRL} after CS goes low may result in the DP8409 interpreting the RASIN as a hidden refresh RASIN if no hidden refresh has occurred in the current RFCK cycle. In this **case, all** RAS outputs would go low for a short time. Thus, it is suggested that when using Mode 5, RASIN should be held high until t_{CSRL} after $\overline{CS}$ goes low if a refresh is not intended. Similarly, CS should be held low for a mini. mum of t_{CSRL} after RASIN returns high when ending the access in Mode 5.

Mode 6 — Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10ns to 15ns) in applications requiring fast access times; RASIN to $\overline{CAS}$ is typically 105ns.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but CASIN (RGCK) is used as CASIN to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 8b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by CASIN to extend the data output valid time from the DRAM to allow the system to read the data. CASIN subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, CASIN should be set high in Mode 6.

There is no internal refresh-request flip-flop in this mode, so any refreshing required must be done by entering Mode 0 or Mode 2.

Mode 7 — Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and BO (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1. EOC is 255; and with B1 = 1 and B0 = 0, EOC is 511 This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and BO set to 11).

Table 3. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

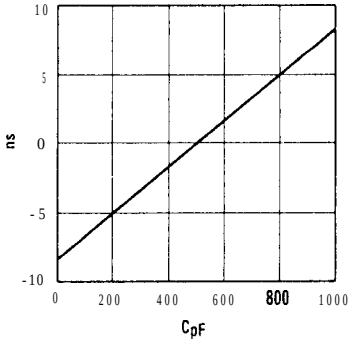


FIGURE 10. Change in Propagation Delay vs. Loading Capacitance Relative to a 500pF Load

Absolute Maximum Ratings (Note 1)

Supply Voltage, Vcc	7.0V
Storage Temperature Range	-65°C to +150°C
Input Voltage	5.5V
Output Current	150mA
Lead Temperature (Soldering, 10 seconds)	300 °C

Operating Conditions

	Min.	Max.	Units
Vcc Supply Voltage	4.75	5.25	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2.6)

symbol----	Parameter	Conditions	Min.	Typ.	Max.	Units
V_C	Input Clamp Voltage	V_{CC} = Min., $I_C = -12mA$		-0.8	-1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ only	$V_{IN} = 2.5V$		2.0	100	µA
I_{IH2}	Input High Current for All Other Inputs'	$V_{IN} = 2.5V$		1.0	50	µA
I_I RSI	Output Load Current for RF I/O	$V_{IN} = 0.5V$, Output High		-1.5	-2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, CAS, $\overline{WE}$	$V_{IN} = 0.5V$, Chip Deselect		-1.5	-2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ only	$V_{IN} = 0.5V$		-0.1	-1.0	mA
I_{IL2}	Input Low Current for All Other Inputs'	$V_{IN} = 0.5V$		-0.05	-0.5	mA
V_{IL}	Input Low Threshold				0.6	V
Input High Threshold			2.0			V
V_{OL1}	Output Low Voltage'	$I_{OL} = 20mA$		0.3	0.5	v
V_{OL2}	Output Low Voltage for RF I/O	$I_{OL} = 10mA$		0.3	0.5	v
V_{OH1}	Output High Voltage'	$I_{OH} = -1$ mA	2.4	3.5		v
V_{OH2}	Output High Voltage for RF I/O	$I_{OH} = -100\mu A$	2.4	3.5		V
I_{1D}	Output High Drive Current'	$V_{OUT} = 0.8V$ (Note 3)		-200		mA
I_{0D}	Output Low Drive Current*	$V_{OUT} = 2.7V$ (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, $\overline{CS} = 2.0V$, Mode 4	-50	1.0	50	µA
	Supply Current	V_{CC} = Max.		250	325	mA

*Except RF I/O Output

Switching Characteristics: DP8409/DP8409-3 $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2. 4. 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0-Q8, C_L = 500pF; $\overline{RAS0}$-$\overline{RAS3}$, C_L = 150pF; $\overline{WE}$, CL = 500pF; $\overline{CAS}$, C_L = 600pF, unless otherwise noted. See Figure 11 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted.

Symbol	Access Parameter	Conditions	8409			8409 – 3			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8b	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	Figure 8a	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	Figures 8a, 8b	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 8a	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 8a, 8b	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 8a		90	120		90	140	ns

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8409			8409 – 3			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 8a, 8b		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 7a, 7b		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	Figures 7a, 7b		40	60		40	70	ns
t_{ASA}	Address Set-up Time to ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{AHA}	Address Hold Time from ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{ADS}	Address Strobe Pulse Width	Figures 7a, 7b, 8a, 8b	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	Figure 8b	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	32	41	58	32	41	67	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	Figure 7a		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	Figures 7a, 7b		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	Figure 7a	10			10			ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100			100			ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figures 2,3,4		47	60		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figures 2, 3		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figures 2, 4		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50pF, Figure 4			95			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50pF, Figure 4			75			75	ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100			100	ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	Figure 9	100			100			ns
T	Period of $\overline{RAS}$ Generator Clock	Figure 3	100			100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	Figure 3	35			40			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	Figure 3	35			40			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	C_L = 50pF, Figure 3		20	30		20	30	ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	C_L = 50pF, Figure 3		50	75		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	Figure 3	50	65	95	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	Figure 3	40	60	85	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	Figure 3	2T			2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrip.	55	80	110	55	80	125	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			40			ns

Switching Characteristics (Cont'd)

Symbol	Refresh Parameter	Conditions	8409			0400 ■ 3			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CSCT}	$\overline{CS}$ High to RFSH Counter **Valid**	Figure 9		55	70		55	75	ns
t_{CSRL}	$\overline{CS}$ Low to Access RASIN Low	See Mode 5 Descrip.	10			15			ns
	TRI-STATE Parameter								
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi.2 from High	C_L = 15 pF, Figures 9, 12 R2 = 1k, S1 open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15 pF, Figures 9, 12, R1 = 1k, S2 open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	Figures 9, 12 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15 pF, Figures 9, 12 R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	Figure 12, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, Figure 12, R2 = 750Ω, S1 open		50	80		50	80	ns

Switching Characteristics: DP8409-2

V_{CC} = 5.0V ± 5%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 66 DRAMs including trace capacitance. These values are: Q0-Q8, C_L = 500 pF; RAS0-RAS3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; CAS, C_L = 600 pF, unless otherwise noted. See Figure 11 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted.

Symbol	Access Parameter	Conditions	8409 – 2						Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	75	100	130				ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	65	90	115				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	40	48	60				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	50	63	80				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		75	100				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b		65	85				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		27	40				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8a		40	65				ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8b	40	54	70				ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	Figure 8a	20						ns
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	Figures 8a, 8b	12						ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 8a	3						ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 8a, 8b	3						ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 8a		80	105				ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 8a, 8b		70	90				ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	20	27	35				ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	15	23	32				ns

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8409 – 2						Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{APDL}	Address Input to Output Low Delay	Figures 7a, 7b, 8a, 8b		25	40				ns
t_{APDH}	Address Input to Output High Delay	Figures 7a, 7b, 8a, 8b		25	40				ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 7a, 7b		40	60				ns
t_{SPDH}	Address Strobe to Address Output High	Figures 7a, 7b		40	60				ns
t_{ASA}	Address Set-up Time to ADS	Figures 7a, 7b, 8a, 8b	15						ns
t_{AHA}	Address Hold Time from ADS	Figures 7a, 7b, 8a, 8b	15						ns
t_{ADS}	Address Strobe Pulse Width	Figures 7a, 7b, 8a, 8b	30						ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	25	30				ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	30	60				ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	Figure 8b	35						ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	32	41	58				ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	25	39	50				ns
t_{RCC}	Column Select to Column Address Valid	Figure 7a		40	58				ns
t_{RCR}	Row Select to Row Address Valid	Figures 7a, 7b		40	58				ns
t_{RHA}	Row Address Held from Column Select	Figure 7a	10						ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100						ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50						ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	35	50	70				ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	30	40	55				ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = Figures 2,3,4		47	80				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figures 2, 3		45	60				ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figures 2, 4		30	55				ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80				ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80				ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50pF, Figure 4			95				ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50pF, Figure 4			75				ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70						ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100				ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	Figure 9	100						ns
T	Period of $\overline{RAS}$ Generator Clock	Figure 3	100						ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	Figure 3	35						ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	Figure 3	35						ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	C_L = 50pF, Figure 3		20	30				ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	CL = 50pF, Figure 3		50	75				ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	Figure 3	50	65	95				ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	Figure 3	40	60	85				ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	Figure 3	2T						ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrtp.	55	80	110				ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	See Mode 1 Descrtp.	35						ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	Figure 9		55	70				ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrtp.	10						ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	6409 = 2						Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	CL= 15pF, Figures 9. 12 R2 = 1 k, S1 open		20	40				ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{LZ}	$\overline{CS}$ High to Address Output H-Z from Low	CL= 15pF, Figures 9, 12 R1 = 1 k, S2 open		25	50				n s
t_{HZH}	CS Low to Control Output High from Hi-Z High	Figures 9, 12 R2 = 750Ω, S1 open		50	80				ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z Hi , from High	C_L = 15pF, Figures 9, 12 R2 = 750Ω, S1 open		40	75				ns
t_{HZL}	CS Low to Control Output Low from HI-7 High	Figure 12. S1, S2 open		45	75				ns
t_{LHZ}	CS High to Control Output Hi-Z Hig from Low	C_L = 15pF, Figure 12, R2 = 750Ω, S1 open		50	60				ns

Input capacitance T_A = 25°C (Notes 2, 6)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance ADS, R/C			6		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed They are not meant to Imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V

Note 3: This test is provided as a monitor of Driver output source and sink current capability Caution should be exercised in testing this parameter. In testing these parameters, a 150Ω resistor should be placed in series with each output under test One output should be tested al a time and test time should not exceed 1 second

Note 4: Input pulse OV to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz, t_{PW} = 200"s Input reference point on AC measurements is 1 5V Output reference points are 2 7V for High and 0.8V for Lo....

Note 5: The load capacitance on RF I/O should not exceed 50pF

Note 6: Applies to all DP8409 versions unless otherwise specified.

Note 7. The DP8409-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.

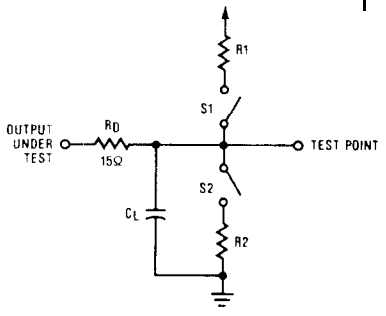


FIGURE 11. **Output Load Circuit**

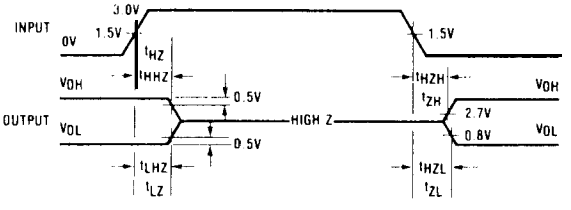


FIGURE 12. **Waveform**

Appendix A:
Overview Of DRAMs And The DRAM Board (continued)

Applications

If external control is preferred, the DP8409 may be used in Mode 0 or 4, as in Figure 6.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 1 and 5 are ideal, as shown in Figure 13a The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8409. Furthermore, two separate $\overline{CAS}$ outputs are also Included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on the input clock of 2 to 10 MHz. Figure 13b shows the general timing diagram for interfacing the DP6409 to different microprocessors using the interface controller DP843X2.

If high-speed access is required, then Modes 5 and 6 produce delays of $\overline{RASIN}$ to $\overline{CAS}$ of 125ns and 105 ns, respectively. Mode 0 may be used for refresh.

If thesystem is complex, requiring automatic access and refresh, burst refresh, and all-banks auto-write, then morecircuitryisrequiredtoselect themode.Thismay be accomplished by utilizing a PAL. The PAL has two functions. One as an address comparator, so that when the desired port address occurs (programmed in the PAL), the comparator gates the data into a latch, where it is connected to the mode pins of the DP6409. Hence the mode of the DP8409 can be changed as desired with one PAL chip merely by addressing the PAL location, and then outputting data to the mode-control pins. In this manner, all the automatic modes may be selected, assigning R/C as RFCK always, and CASIN as RGCK always. The output from RF I/O may be used as End-of. Count to an interrupt, or Refresh Request to HOLD or BUS REQUEST. A complex system may use Modes 5and 1 for automatic access and refresh, Modes 3a and 7 for system initialization, and Mode 2 (auto-burst refresh) before and after DMA.

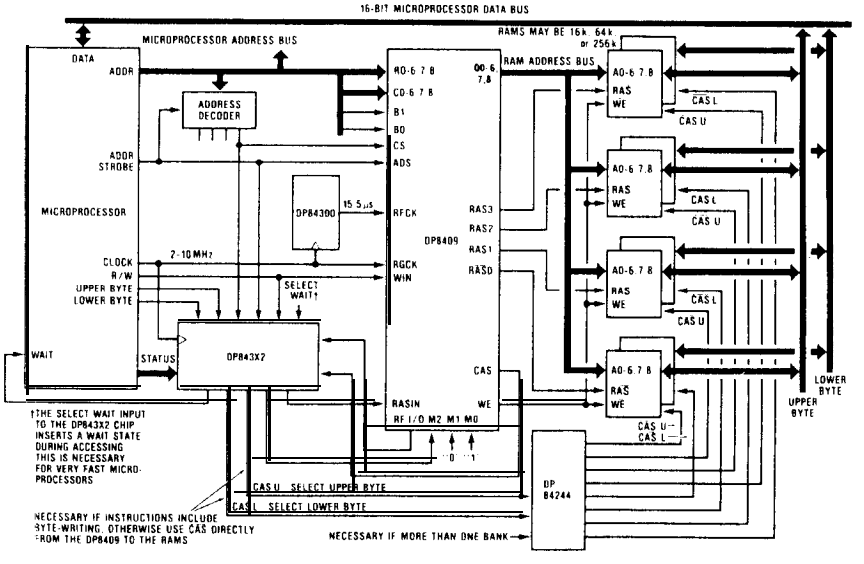


FIGURE 13a. Connecting the DP8409 Between the 16-bit Microprocessor and Memory

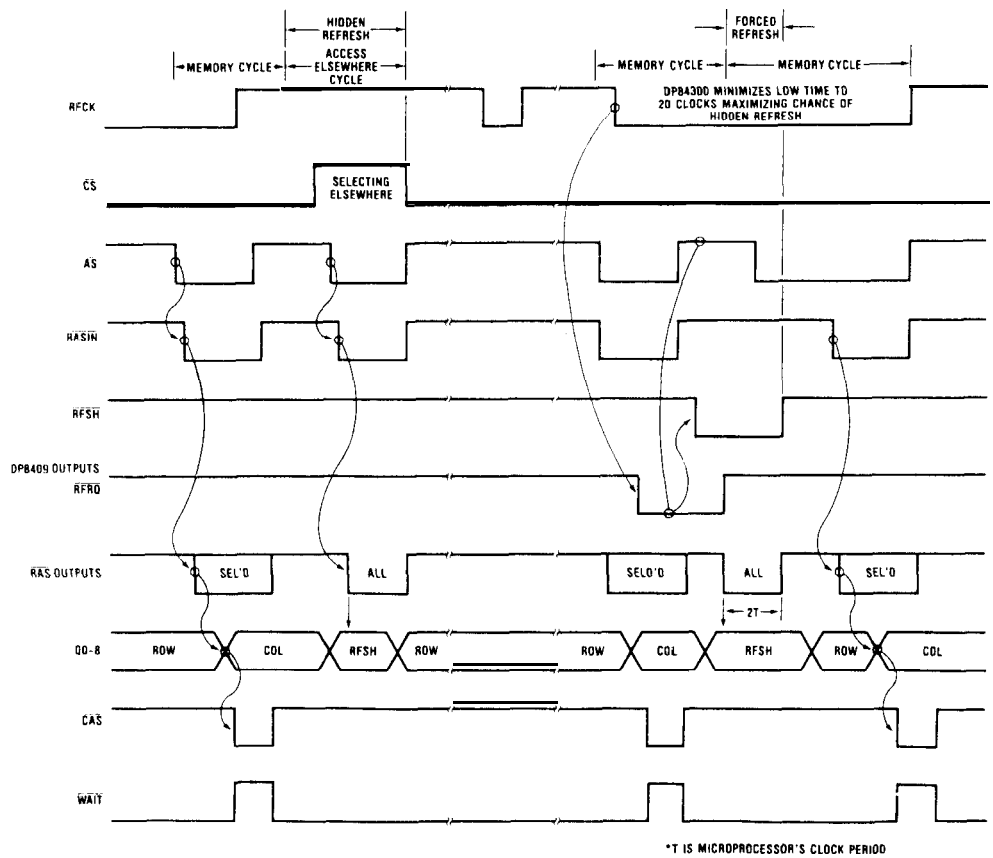
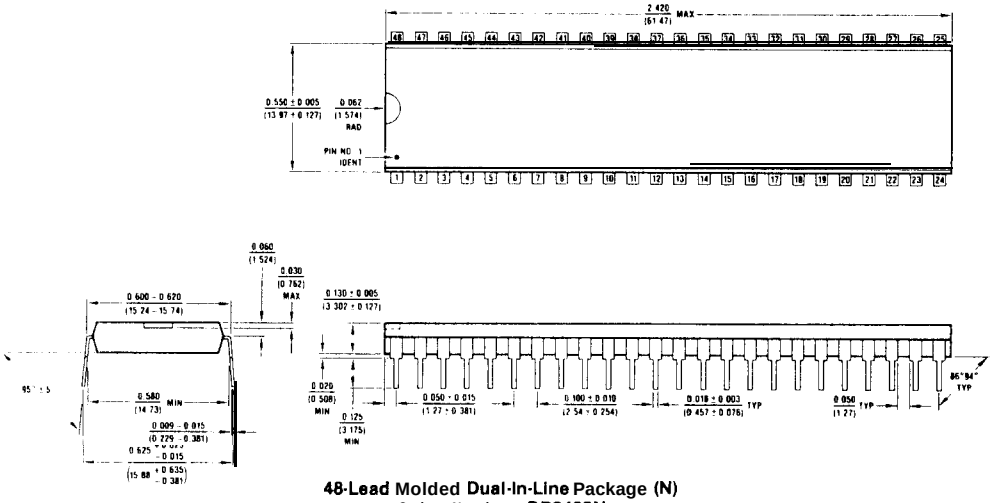


FIGURE 13b. **DP8409** Auto Refresh

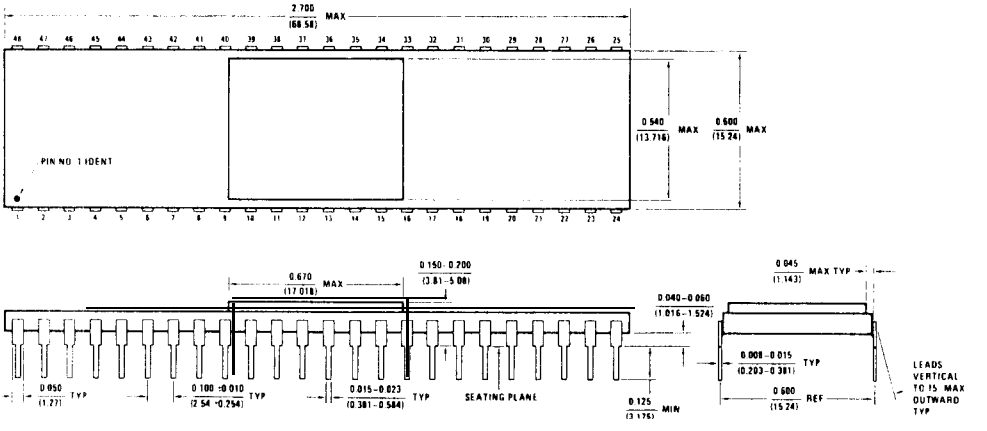
Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

DP8409 Multi-Mode Dynamic RAM Controller/Driver

Physical Dimensions (inches/millimeters)



48-Lead Molded Dual-In-Line Package (N)
Order Number **DP8409N**
or Order Number **DP8409N-3**
NS Package **N48A**



48-Lead Dual-In-Line Package (D)
Order Number **DP8409D**
NS Package **D48A**

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Technical Data For The Hitachi HM 4864 DRAM

HM4864-2, HM4864-3
HM4864P-2, HM4864P-3

65536- word × l-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by l-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

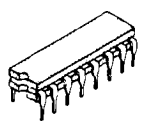
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and RAS-only refresh.

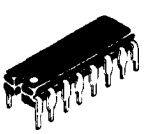
Proper control of the clock inputs ($\overline{RAS}$, CAS, and $\overline{WE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

HM4864-2, HM4864-3



(DG-16A)

HM4864P-2, HM4864P-3

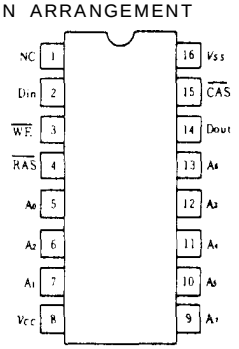


(DP-16)

■ FEATURES

- **Recognized industry standard 16-pin configuration**
- **150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)**
- **200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)**
- **Single power supply of +5V±10% with a built-in V_{BB} generator**
- **Low Power; 330 mW active. 20 mW standby (max)**
- **The inputs TTL compatible, low capacitance, and protected against static charge**
- **Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary**
- **Common I/O capability using "early write" operation**
- **Read-Modify-Write, RAS-only refresh, and Page-mode capability**
- **128 refresh cycle**

■ PIN ARRANGEMENT



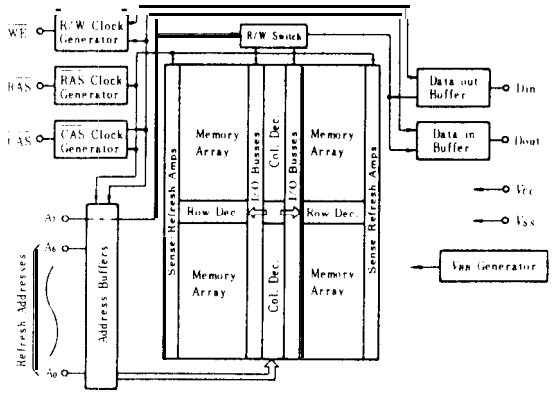
(Top View)

A_0-A_7	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5V)
V_{SS}	Ground
A_0-A_6	Refresh Address Strobe

Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . . -65 to +150°C
Short-circuit Output Current . 50 mA
Power Dissipation . . . , ... 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = min.)	I_{CC1}	–	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, Dout = High Impedance)	I_{CC2}	–	3.5	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}	–	45	mA	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = min.	I_{CC4}	–	45	mA	2, 4
INPUT LEAKAGE Input Leakage Current, any Input (V_{in} = 0 to +6.5V, all other pins not under test = 0V)	I_{LI}	-10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, V_{out} = 0 to +5.5V)	I_{LO}	-10	10	μA	3
OUTPUT LEVELS Output High Logic 1 Voltage (I_{OH} = -5mA Output Low Logic 0 Voltage (I_{OL} = 4.2mA)	V_{OH} V_{OL}	2.4 0	V_{CC} 0.4	V V	

NOTES
1. All voltages referenced to V_{SS}.
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (A_0-A_7, Din)	C_{in1}	–	7	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	–	10	pF	1
Output Capacitance (Dout)	C_{out}	–	7	pF	1, 2

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1, 2]

(Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM4864-2/P-2		HM4864-3/P-3		Unit	Notes
		min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	270	—	335	—	ns	
Read-Write Cycle Time	t_{RWC}	270	—	335	—	ns	
Page Mode Cycle Time	t_{PC}	170	—	225	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	150	—	200	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	100	—	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	—	135	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	—	135	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	—	200	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	65	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	—	−20	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	ns	
Column Address Set-up Time	t_{ASC}	−10	—	−10	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	95	—	120	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	—	120	—	ns	
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	55	—	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	—	120	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Refresh Period	t_{REF}	—	2	—	2	ms	
Write Command Set-up Time	t_{WCS}	−20	—	−20	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	80	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110	—	145	—	ns	10
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	ns	

NOTES

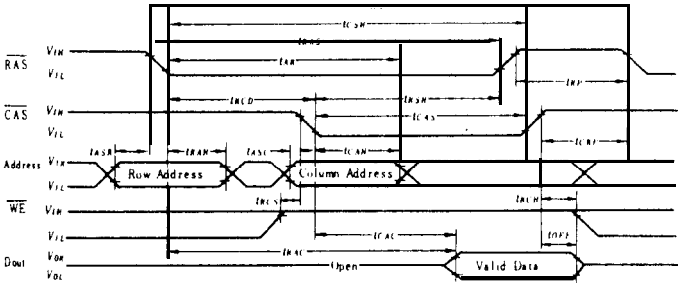
1. AC measurements assume t_T = 5ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
9. These parameters are reference to CAS leading edge in ﾘﾄｽﾗｲﾄ write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

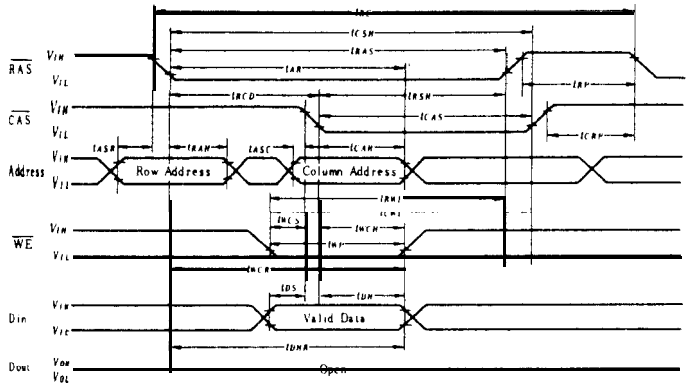
HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

■ TIMING WAVEFORMS

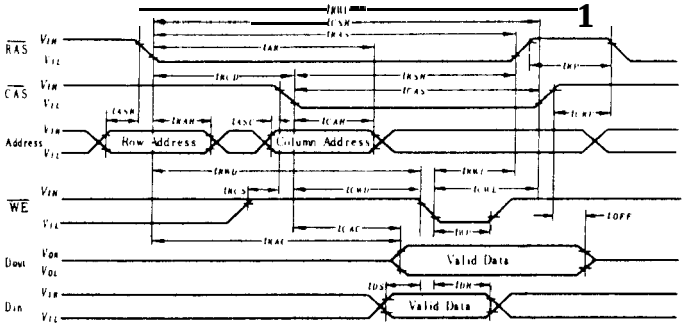
● **READ CYCLE**



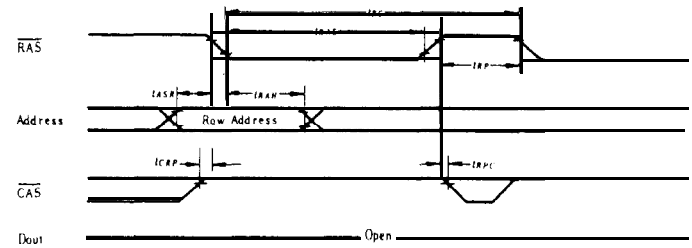
● **WRITE CYCLE**



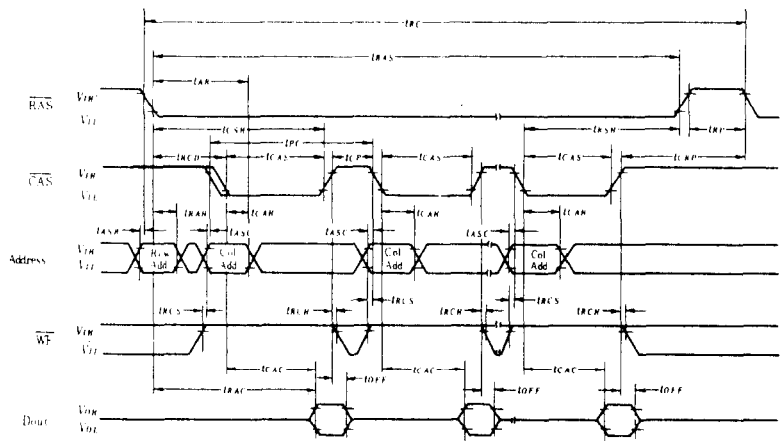
● **READ-WRITE/READ-MODIFY-WRITE CYCLE**



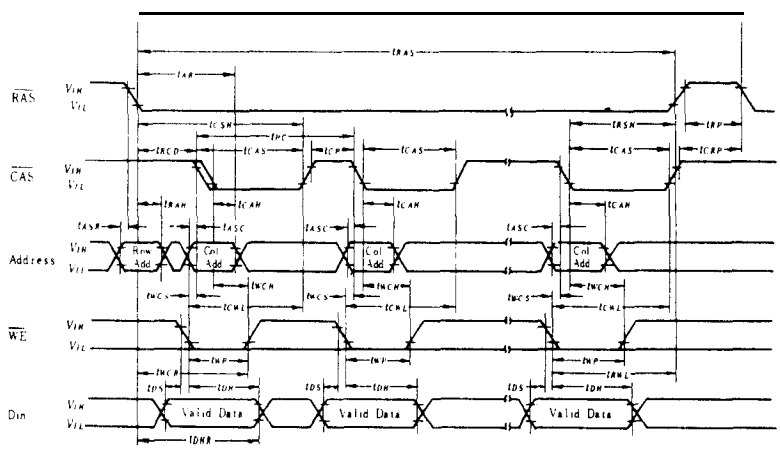
●"RAS-ONLY" REFRESH CYCLE



●PAGE MODE READ CYCLE



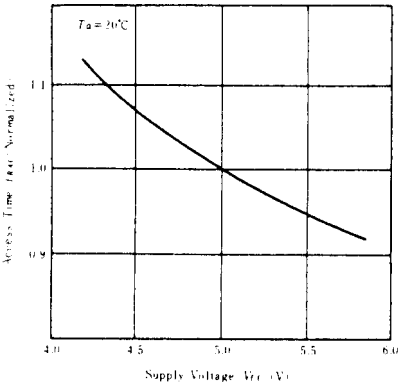
●PAGE MODE WRITE CYCLE



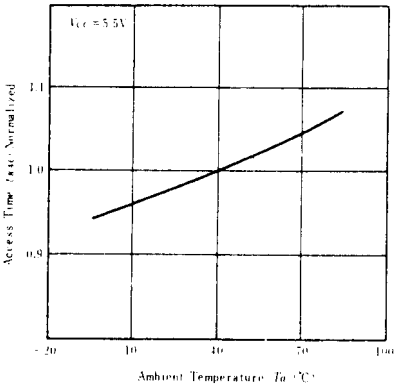
Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

■ **TYPICAL CHARACTERISTICS**

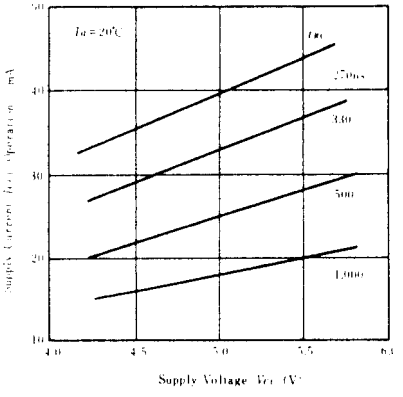
ACCESS TIME
vs. SUPPLY VOLTAGE



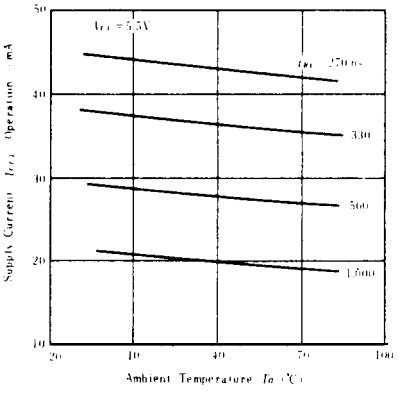
ACCESS TIME
vs. AMBIENT TEMPERATURE



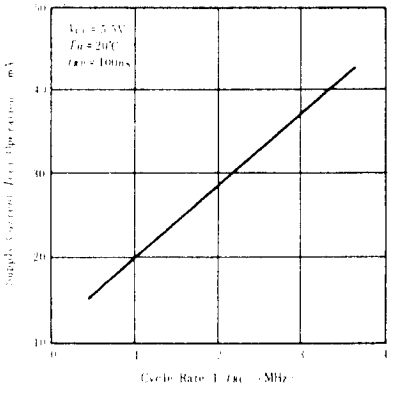
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



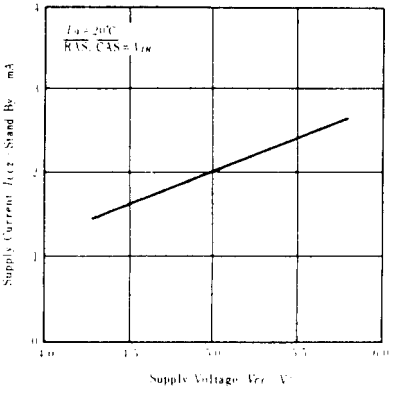
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



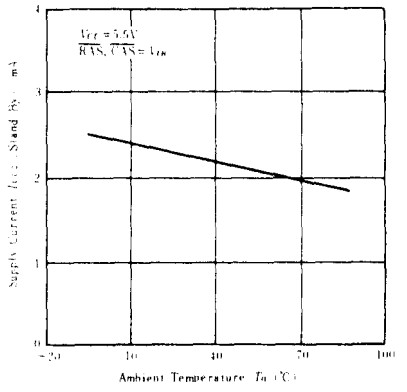
SUPPLY CURRENT
vs. CYCLE RATE



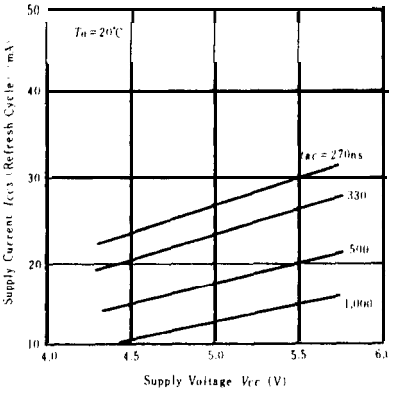
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



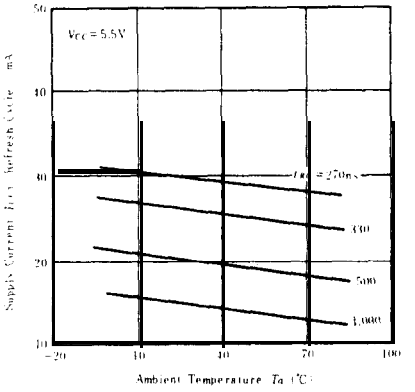
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



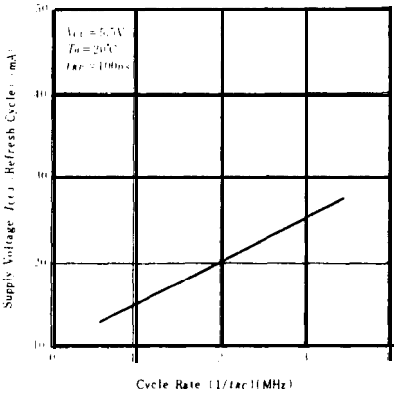
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



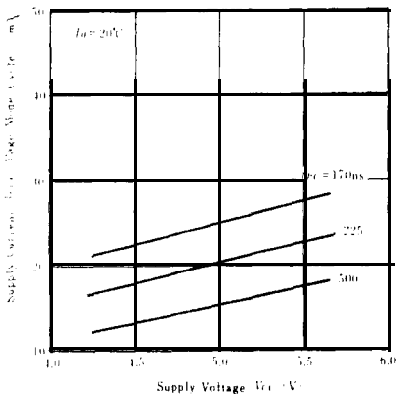
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



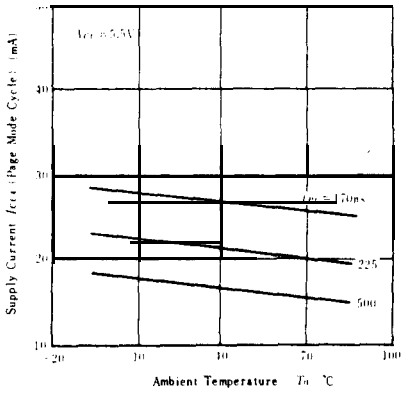
SUPPLY CURRENT
vs. CYCLE RATE



SUPPLY CURRENT
vs. SUPPLY VOLTAGE



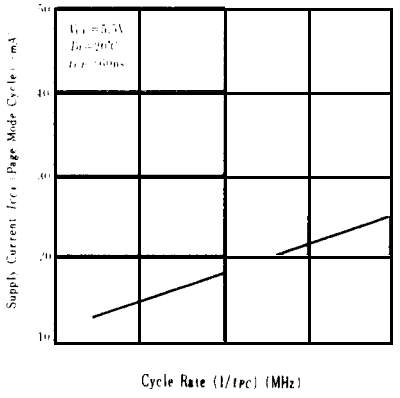
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



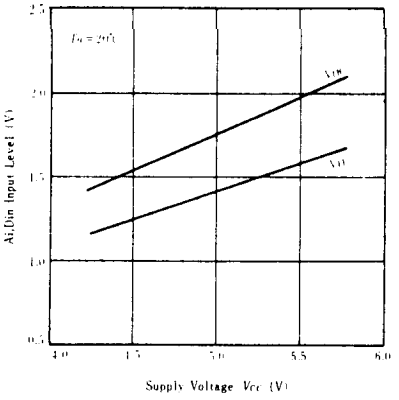
Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

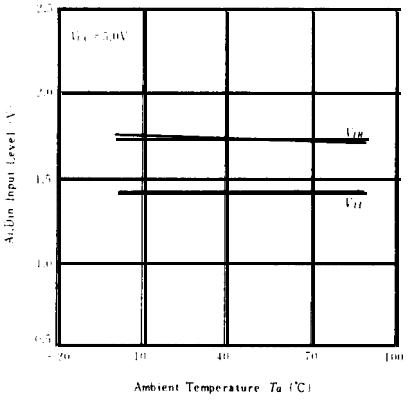
SUPPLY CURRENT
vs. CYCLE RATE



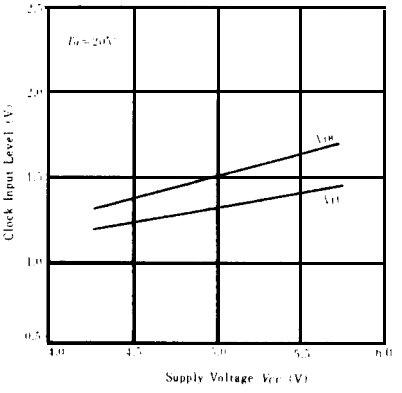
INPUT LEVEL
vs. SUPPLY VOLTAGE



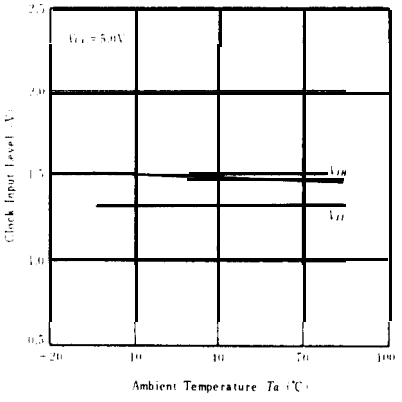
INPUT LEVEL
vs. AMBIENT TEMPERATURE

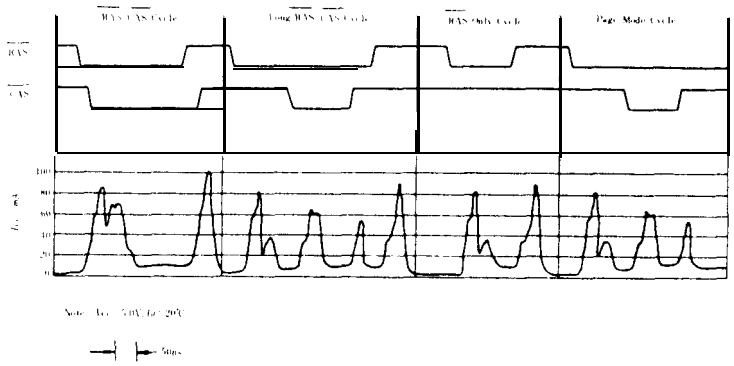


CLOCK INPUT LEVEL
vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL
vs. AMBIENT TEMPERATURE





APPLICATION INFORMATION

● POWER ON

An initial pause of 500 μs is required after power-up and a minimum of eight (8) initialization cycle, (any combination of cycles containing a $\overline{RAS}$ clock such as m-only refresh) must follow an initial pause.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of V_{CC}, as shown in Fig. 1.

● READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of RAS-on is controlled by parameter t_{ASR}.

Following the time when RAS reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH}. Following this interval, the address can be changed from row address to column address. When the column address is stable, $\overline{CAS}$ can be turned on. The leading edge of CAS is controlled by parameter t_{RCD}. The basic limit on the CAS leading edge is that CAS can not start until the column address is stable, and this is controlled by parameter t_{ASC} The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH}. Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than t_{RCD} (max), the access time from RAS will be increased by the time which t_{RCD} exceeds t_{RCD} (max).

Following the time when CAS reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC} ·access time from $\overline{CAS}$.

The access time from RAS–t_{RAC}–is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of t_{RAC} is derived as the sum Of t_{RCD} (max) and t_{CAC}.

The selected output data is held valid internally until CAS becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF}.

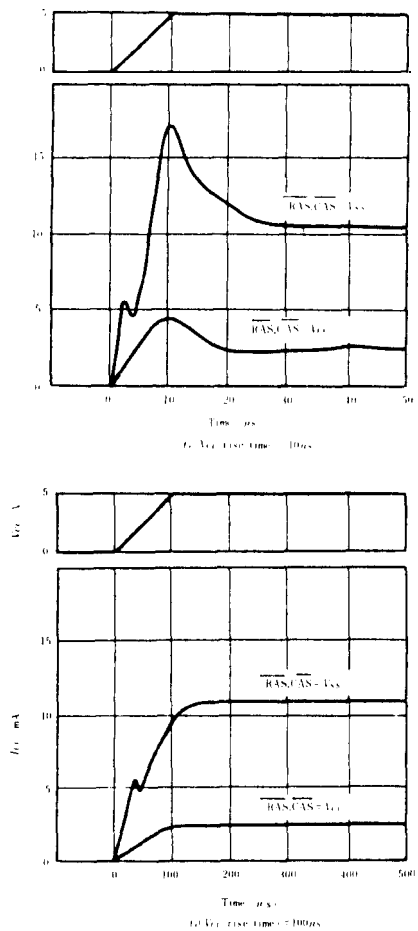


Fig.1 I_{cc} vs. V_{cc} during power up.

Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

- **WRITE CYCLE**

A write cycle is performed by bringing $\overline{WE}$ low before or during $\overline{CAS}$-on.

different write cycles can be defined as;

Write cycle-Writedata are available at the beginning of the $\overline{CAS}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{WE}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{WE}$ reaches its low level, $\overline{WE}$ must be held stable long enough to be captured. This $\overline{WE}$-on pulse deration is called t_{WP}. The time required to capture write data in a latch is called t_{DH}. This cycle is called an "early write".

Read Write cycle-This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

$\overline{WE}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{WE}$ become critical path signals for determining cycle time.

. **CLOCK-OFF TIMING**

$\overline{RAS}$ and $\overline{CAS}$ must stay on for Dout stabilized to valid data. In the case of CAS, this is controlled by parameter t_{CAS} (min).

In the case of RAS, this is controlled by parameter t_{CAS} (min). Following the end of $\overline{RAS}$, $\overline{CAS}$ must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP}. Normally $\overline{CAS}$ is not required to be off for minimum time of t_{CRP}. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time.

. **DATA OUTPUT**

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CAS}$ is high, Dout is in a high impedance state. When $\overline{CAS}$ is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

- **REFRESH**

Refresh of the HM4864 is accomplished by per. forming a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{IL} or V_{IH} is permitted for A7. Any cycle in which $\overline{RAS}$ signal occurs refreshes the entire selected row. $\overline{RAS}$-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

. **PAGE MODE**

Page mode operation allows faster successive memo. ry operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining RAS at a logic low throughout all successive CAS memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

Dram Board ROM Listings

1) Memory test to allow hidden refreshes is in locations 4000H through 4007H.

2) Routine to transfer code from ROM to DRAM is in locations 4020H through 403DH. To use, perform the following steps on the HP 5036A:

Fetch address 0800H and store the starting address of the code section to be transferred in locations 0800H and 080 1 H.

Fetch address 0802H and store the ending address of the code section to be transferred in locations 0802H and 0803H.

Fetch address 0805H and store the start address in DRAM where the program is to be moved to. DRAM addresses start at 8000H.

Fetch address 4020H (start of the transfer routine) and press the RUN key on the 5036A. The display on the 5036A will display 'uLAb UP'. The code section has been transferred. *Note: this routine will nor perform linking.*

3) Routine to consecutively select memory, I/O, and control ports is in locations 4050H through 4068H. Program will run until stopped with the RESET key on the 5036A.

4) Routine in locations 4070H through 407AH monitors the DIP switch on the input port of the 5036A and transfers the complement to the output port.

5) Locations 4100H through 4142H contain a memory test routine for testing the operation of the DRAM and the ability of the DRAM controller to perform forced refreshes.

Appendix A:
Overview Of DRAMs And The DRAM BOARD (continued)

Listing

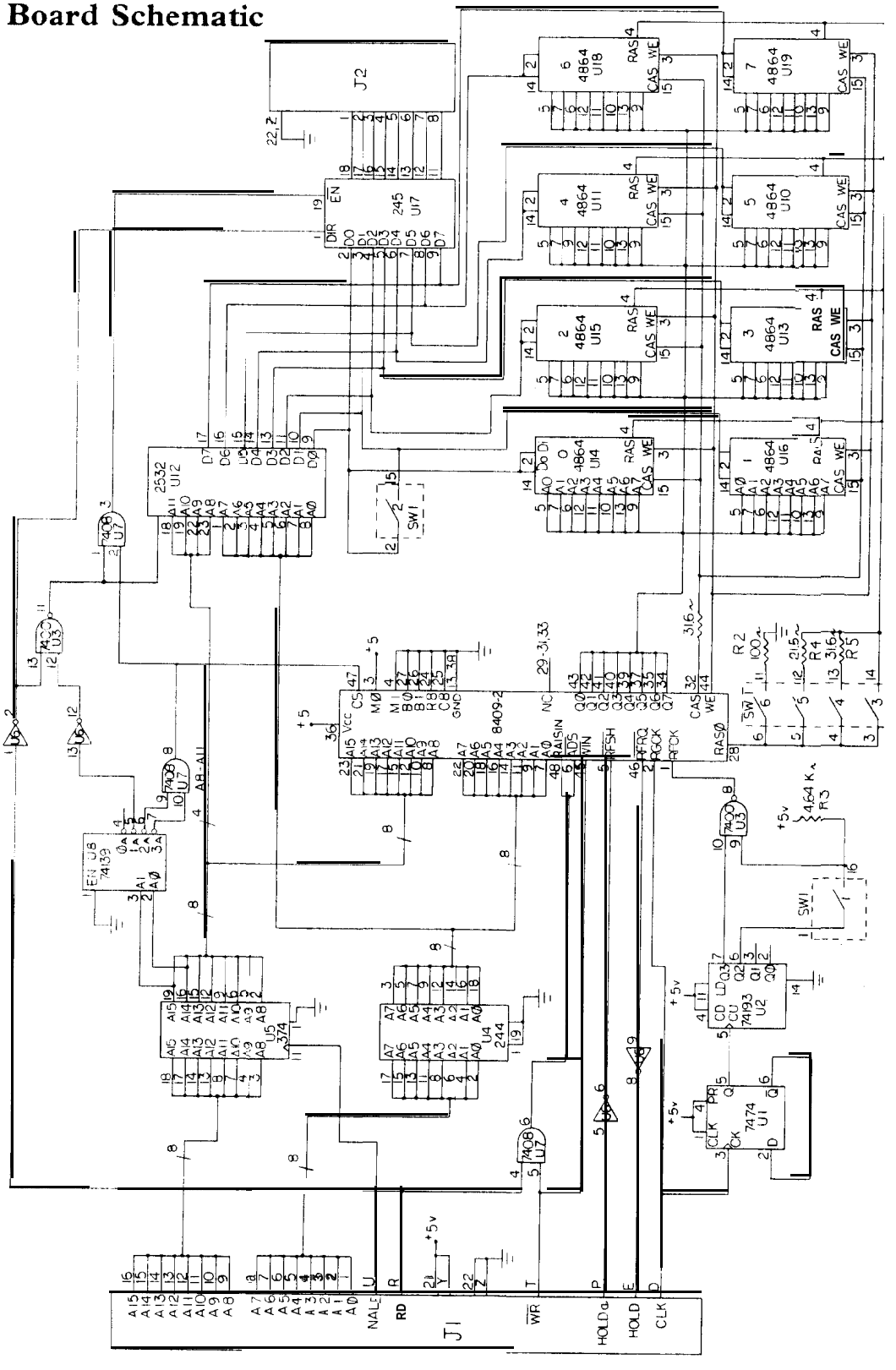
```
4000 00          NOP
4001 00          h-01'
4002 00          NOP
4003 00          NOP
4004 00          NOP
4005 00          NOP
4006 C9          RET

4020 2A0800      LHLD    0800H
4023 EB          XCHG
4024 2A0804      LHLD    0804H
4027 1B          DCX     D
4028 2B          DCX     H
4029 13    LBLIO INX     D
402A 23          INX     H
402B IA          LDAX    D
402C 77          MOV     M,A
402D 3A0802      LDA     0802H
40.30 AB         XRA     E
403 1C24029      JNZ     LBLIO
4034 3A0803      LDA     0803H
4037 AA          XRA     D
4038 C24029      JNZ     LBLIO
403B C30038      JMP     0038H

4050 3A0000 LBL11 LDA    0000H
4053 321000      STA     1000H
4056 3A1800      LDA     1800H
4059 3A2000      LDA     2000H
405C 322800      STA     2800H
405F 323000      STA     3000H
4062 323800      STA     3800H
4065 C34050      JMP     4050H

4070 3A2000 LBL12 LDA    2000H
4073 2F          CMA
4074 323000      STA     3000H
4077 C34070      JMP     LBL12
                 ORG 8000H (LOCATED AT 4100H)
8000 218050      LX1     H,8050H
8003 3E55  LBL1  MVI     A,055H
8005 77          MOV     M,A
8006 23          INX     H
8007 3EFF        MVI     A,OFFH
8009 BD          CMP     L
800A CA8010      JZ      LBL2
800D C38003      JMP     LBL1
8010 BC    LBL2  CMP     H
8011 C28003      JNZ     LBL1
8014 3655        MVI     M,055H
8016 3E55        MVI     A,055H
8018 218050 LBL3 LX1     H,8050H
801B BE    LBL4  CMP     M
801C C28040      JNZ     LBL5
801F 47          MOV     B,A
8020 2F          CMA
8021 77          MOV     M,A
8022 23          INX     H
8023 7C          MOV     A,H
8024 B5          ORA     L
8025 78          MOV     A,B
8026 C2801B      JNZ     LBL4
8029 1608        MVI     D,008H
802B 21FFFF LBL6 LX1     H,FFFFH
802E 2B    LBL7  DCX     H
802F 7C          MOV     A,H
8030 B5          ORA     L
8031 C2802E      JNZ     LBL7
8034 15          DCR     D
8035 C2802B      JNZ     LBL6
8038 78          MOV     A,B
8039 2F          CMA
803A CD4000      CALL    4000H
803D C38018      JMP     LBL3
8040 C30038      JMP     0038H
```

DRAM Board Schematic



Appendix B:
Overview Of FORMAT/TRACE Menus

Overview Of Analog FORMAT/TRACE Menus

This section is intended for reference and to acquaint you briefly with the FORMAT and TRACE menus and their functions. For more information, consult the HP 1631A/D operating and programming manual.

FORMAT (analog)

Press the FORMAT key, which is one of the six along the top of the keyboard. This menu is used to set the format specifications for each measurement.

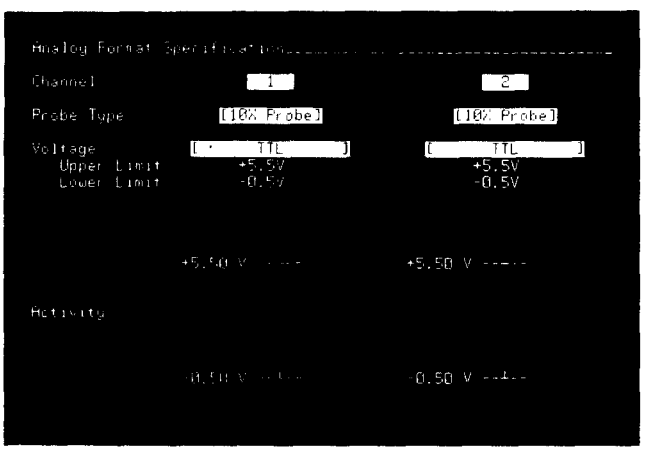


Figure 51

Notice the two label fields at the top with the numbers 1 and 2. These are labels for the analog channels. Up to five letters and/or numbers can be entered in these fields from the keyboard as channel/signal names.

Below the label fields are two fields that allow you to select the probe type you are using. Since these fields are surrounded by brackets [ ], they are changed with the PREV[ ] or NEXT[ ] key. The possible choices here are [1X], [10X], and [50X]. Each has its own advisory which tells you the full scale voltage.

Moving down, the next set of fields is used to select the display voltage range. These are changed by the PREV[ ]/ NEXT[ ] keys. You can select [TTL] or [ECL] presets, or a user-specified range up to a full scale maximum of 25 volts. When the user-specified voltage range is selected, fields are displayed below the label for setting upper and lower voltage ranges.

The last bit of information in this menu is given by the ACTIVITY area in the lower half of the screen. These areas graphically display the range of voltage seen by the probe tip. This gives you a quick indication of whether the node to which you are connected is active. Also note the arrows above and below the activity indicator for channel 1 in figure 5 1. These appear if the node to which you are connected has excursions above or below the set limits.

TRACE (analog)

Press the TRACE key, which is one of the six along the top of the keyboard. This menu is used to set the trace specifications for each measurement.

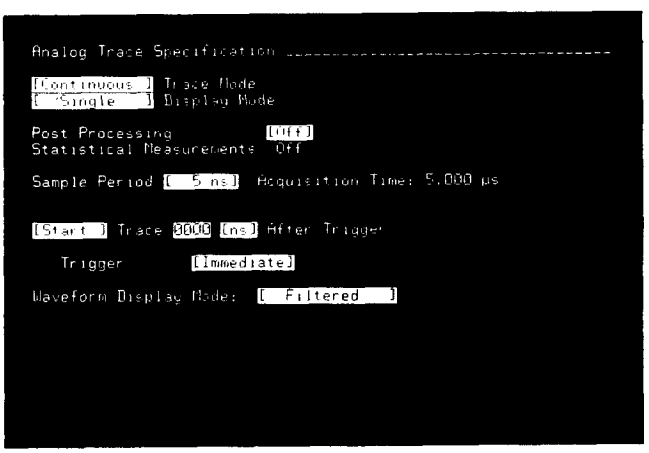


Figure 52

The first field in the menu is the trace mode. The two modes are [Continuous] and [Single]. Continuous is simply a series of single-shot acquisitions. Each time the analyzer meets the specified trace condition (trace = trigger + delay), it captures the data and goes on to another acquisition. In single mode, the first time the analyzer sees data that meets its trace specification, it fills its internal memory, stops, and displays the data.

Immediately below the trace mode field is the display mode field. Two possibilities are available for this field: [Single] and [Cumulative]. In single, each acquisition is displayed individually and then erased when the next acquisition is captured. Cumulative is essentially infinite persistence. Each acquisition is captured and displayed; the display is not erased when a new acquisition is put on screen.

Appendix B:
Overview Of FORMAT/TRACE Menus (continued)

Next is the post-processing selection field. This enables or disables the post-processing capability of the oscilloscope section of the analyzer. Post-processing is a new measurement concept in logic analysis and its menus are covered in measurement 4.

Immediately below the post-processing field is a field labeled Statistical Measurements. When post-processing is off, the statistical measurements field is disabled. When post-processing is turned on, the statistical measurements field is enabled so you can choose the measurement you want.

Below the post-processing and statistical measurements fields is the sample period field. This field allows you to select the sample period for the NEXT[ ]/PREV[ ] keys for the analog section from 5 ns to 500 ms in a l-2-5 sequence.

The next field below the sample period is used to tell the analyzer how to store data in its internal memory. The field labeled [Start] can be changed using the PREV[ ]/NEXT[ ] keys to [Center] or [End]. In start, the analyzer finds the selected tracepoint, and fills its memory with data until it is full. If the field is changed to center, the analyzer places the selected tracepoint in the center of its memory and stores data on either side (before and after). In the end trace mode, the analyzer stops immediately upon finding its tracepoint. This means that the memory is filled with data that occurred before the tracepoint.

'The delay field, immediately following the [Start] field, allows you to delay capture of data by a specified amount after the trigger point. Thus, tracepoint = trigger + delay.

'The trigger field specifies the trigger point that the analyzer will search for. It can be specified as [Immediate], which means that it captures data as soon as you press the RIJN key, or set to a specific channel, edge, and trigger level. Channels can be [1], [2], or [External]. Edges are [Rising] or [Falling], and the trigger level can be set to any level within the selected voltage range as selected in the Format menu.

The Waveform Display Mode, the last field in the menu, gives you two choices: [Filtered], and [Straight Line]. In the filtered mode, the HP 1631A/D uses its software interpolator and inserts software-generated points between actual data points. In the straight line mode, the HP 1631A/D displays only actual data points and connects them with straight lines.

Overview Of Timing FORMAT/TRACE Menus

This section is intended for reference and to acquaint you with the FORMAT and TRACE menus and their functions For more information, consult the HP 1631A/D operating and programming manual.

FORMAT (timing)

Press the FORMAT key, which is one of six along the top of the keyboard. This menu is used to set the format specifications for each measurement.

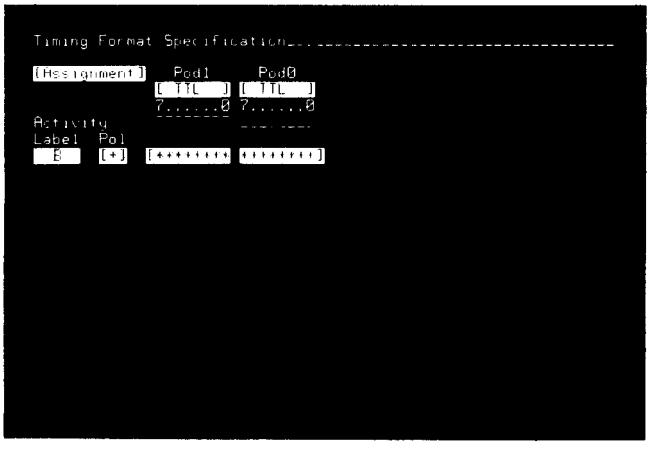


Figure 53

There are two menus for timing format. The first is displayed in figure 53 and is denoted by the [Assignment] field directly below the format label at the top of the menu. We will discuss the [Assignment] menu first.

Depending on whether the analyzer is configured with eight or 16 timing channels, the assignment menu shows Pod 1 and Pod 0. If configured with eight channels, only pod 0 appears. If configured with 16 channels of timing, pods I and 0 appear.

Under each pod assignment label is a field that allows you to select the threshold voltage. Default value is [TTL], but [ECL] or a user-specified value can be selected.

Just under each pod label, there are activity indicators. When the analyzer is stopped, these indicators show the current state of each bit. If there is signal activity on a line, a double-ended arrow is (displayed. If there is a constant high or low on the line, a bar is displayed, as shown in figure 53.

The field to the left with the "B" in it is a label field for the signal lines. You can have up to eight of these labels, each with a five-letter name that is entered from the keyboard. For instance, if you have all eight lines from pod 1 connected to the data bus, you can label those eight lines DATA with the label field, as shown in figure 54.

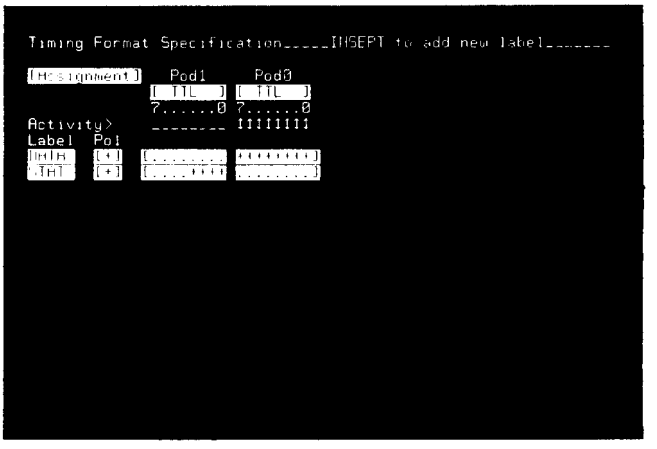


Figure 54

Assignment of a bit or bits of a pod to a particular signal is accomplished via the bracketed fields to the right of each label. Each bit with an asterisk is assigned to the label to the left of it. More than one bit may be assigned to each label. In addition, if more than one bit is assigned to a label, the HP 1631A/D will automatically number them in the timing diagram, starting at 0. This is shown in the timing waveform diagram photo (figure 55).

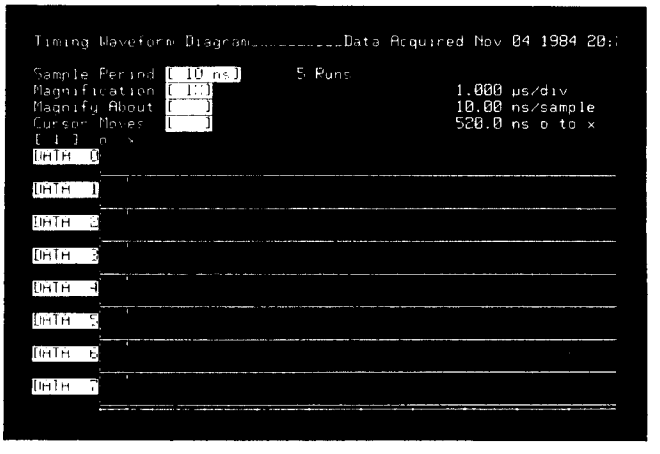


Figure 55

Appendix B:
Overview Of FORMAT/TRACE Menus (continued)

Move the cursor to the [Assignment] field and press NEXT[ ] or PREV[ ]. This puts the analyzer into the second timing format specification menu. This second timing format menu is for setting the user base. User base is a convenience that allows you to label particular bit combinations as appropriate. Notice the number columns at the left in the menu. These relate to the bit assignments in the [Assignment] menu. Suppose you have listed pod bits O-3 as status lines in the assignment menu. Particular patterns of these bits mran certain things in your system; a 101 may mean that the system is doing a memory read. Rather than having to decode a 101 in the data listing, we can label 101 in the user base as MEMRD, as shown. This makes the data listing for timing much easier to read.

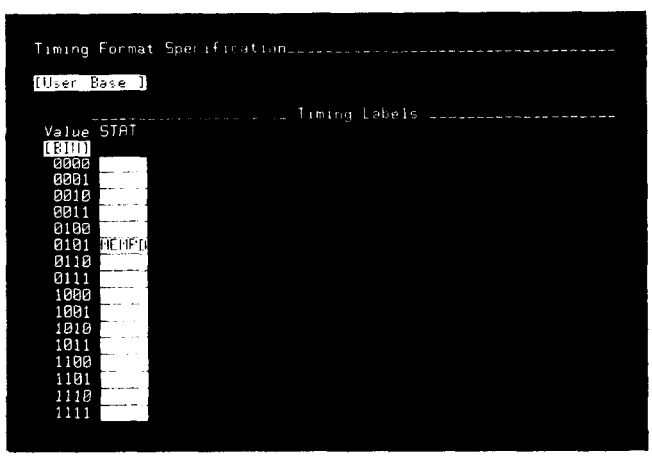


Figure 56

'I-RACE (timing)

Press the TRACE key, which is one of six along the top of the keyboard. This allows you to set the trace specifications for timing measurements.

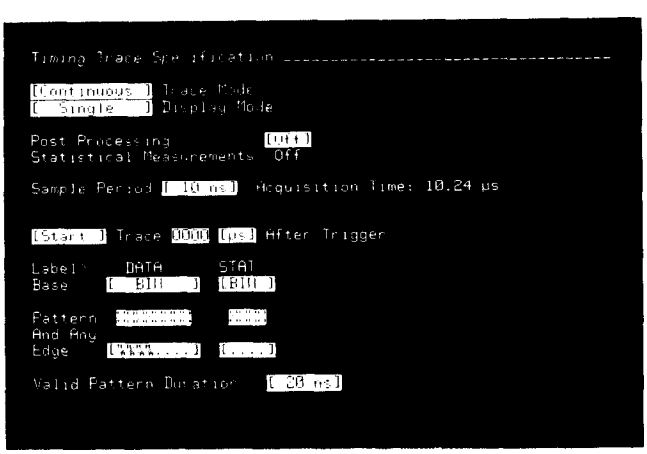


Figure 57

The first two fields, Trace Mode and Display Mode, are the same as for analog trace. The Trace Mode field selects either [Single] or [Continuous] tracing, where continuous is a series of single acquisitions. Each time the analyzer meets the specified trace condition (trace=trigger+delay), it captures the data and goes on to another acquisition. In single mode, the first time the analyzer sees data that meets its trace specification, it fills its internal memory and stops.

The Display Mode has two possibilities: [Single] and [Cumulative]. In single, each acquisition is displayed individually and then erased when the next acquisition is captured. Cumulative is essentially a display with infinite persistence. Each acquisition is captured and displayed; the display is not erased when a new acquisition is put on screen.

Next is the post processing-selection field. This enables of disables the post-processing capability of the timing analyzer. Post processing and its menu are covered in the measurements of this section.

Immediately below the post-processing field is one labeled Statistical Measurements. When post-processing is off, the statistical measurements field is disabled. When post-processing is turned on, the statistical measurements field is enabled so you can choose them. The analyzer must be in continuous trace mode when using statistical measurements.

Below the post-processing and statistical measurements fields is the sample period field. This field allows you to select the sample period for the timing section from 10 ns to 500ms in a l-2-5 sequence.

The next field below the sample period is used to tell the analyzer how to store data in its internal memory. The field labeled [Start] can be changed using the PREV[ ]/NEXT[ ] keys to [Center] or [End]. In start, the analyzer finds the selected tracepoint and then fills its memory with data until it is full. If the field is changed to center, the analyzer places the selected tracepoint in the center of its memory and stores data on either side (before and after). In the end trace mode, the analyzer stops immediately upon finding its tracepoint. This means that the memory is filled with data that occurred before the tracepoint.

The Label field displays all names entered in the format specification menu. Data under each label can be displayed in binary, octal, decimal, hexidecimal, or ASCII, as chosen by the Base field. Each label can be displayed in a different base, if desired.

The Pattern field allows you to set the pattern that the analyzer is to look for. It is analogous to setting the trigger edge and level on an oscilloscope. Since a timing analyzer doesn't look for a trigger level, there is no provision for setting it. Instead, you set a pattern of 1s and 0s and edges or glitches for the analyzer to recognize as its trigger. Measurements in the timing section of this guide deal with this in more detail.

The last field in the menu is Valid Pattern Duration. This field tells the timing analyzer the amount of time the trigger pattern has to last for it to recognize it as a valid trigger. This helps prevent the HP 1631A/D from triggering on transient patterns, or momentary fluctuations that may cross the logic threshold. Obviously, pattern duration checks only for levels and not edges or glitches.

Appendix B:
Overview Of FORMAT/TRACE Menus (continued)

Overview Of State FORMAT/TRACE Menus

This section is intended for reference and to acquaint you with the FORMAT and TRACE menus and their functions For more information, consult the HP 1631A/D operating and programming manual.

FORMAT (state)

Press the FORMAT kev, which is one of the six along the top of the keyboard. This menu is used to set the format specifications for each measurement.

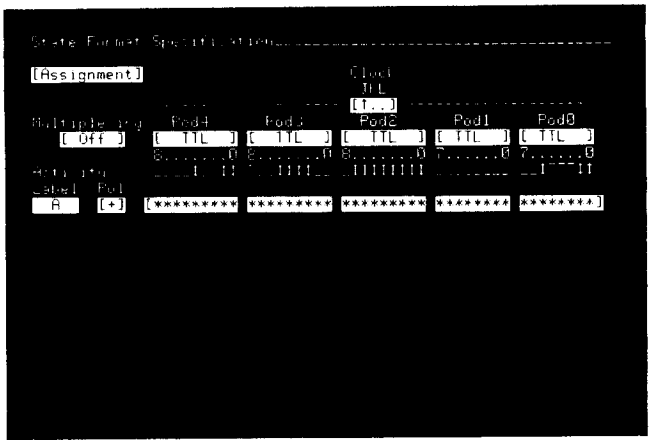


Figure 58

'There are three menus for state format. The first is displayed in figure 58 and is denoted by the [Assignment] field directly below the format label at the top of the menu. We will discuss the [Assignment] menu first.

Depending on whether the analyzer is configured with 43, 35, or 27 state channels, the assignment menu will show Pods 0 through 4. If configured with 43 channels, all five pods are displayed. If 35 channels are chosen, only pods 1 through 4 are shown, with pod 0 committed to timing. If 27 channels are selected, pods 2 through 5 are for state, while channels 0 and] are for timing.

Under each pod assignment label is a field that allows you to choose the threshold voltage. Default value is [TTL], but [ECL] or a user-specified value can be selected.

Just under each pod label are activity indicators. When the analyzer is stopped, these indicators show the current state of each bit. If there is signal activity on a line, a double-ended arrow is displayed. If there is a constant high or low on the line, a bar will be displayed, as shown in the example format menu above.

The field to the left with the "A" in it is the label field for the signal lines. You can have up to eight of these labels, each with a five-letter name that is entered from the keyboard. For instance, if you have 16 lines from pods 2 and 3 connected to the address bus, you can label these 16 lines ADDR with the label field, as shown in figure 59.

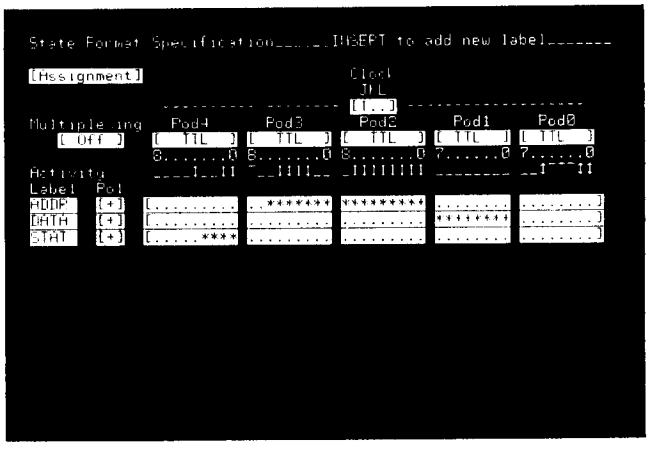


Figure 59

Assignment of a bit or bits of a pod to a particular signal is accomplished via the bracketed fields to the right of each label. Each bit with an asterisk is assigned to the label to the left of it. More than one bit may be assigned to each label. Also, each bit can be assigned to more than one label.

Move the cursor to the [Assignment] field and press the PREV[ ] key. This puts the analyzer into the second state format specification menu. This second state format menu is for setting the user base. User base is a convenience that allows you to label particular bit combinations as appropriate. Notice in the menu the number columns at the left. These relate to the bit assignments in the [Assignment] menu. Suppose you have listed pod bits O-3 as status lines in the assignment menu. Particuar patterns of these bits mean certain things in your system: a 011 may mean that the system is doing an opcode fetch. Rather than having to decode a 011 in the state listing, we can label 011 in the user base as OPFCH, as shown in figure 60. This makes the data listing for state analysis much easier to read.

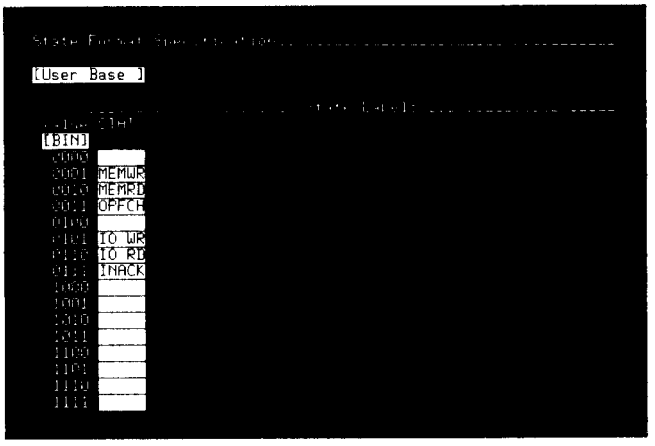


Figure 60

Move the cursor to the [User Base] field and press the PREV[] key. You are now in the third format menu for state analysis. This menu, [Relocation], allows you to input certain address ranges for assembly code routines, and name them. Instead of having to remember the ranges for these routines when setting up a trace specification, the analyzer gives you the option of cycling through the names set with the NEXT[ ]/PREV[ ] keys.

TRACE **(state)**

Press the TRACE key, which is one of the six along the top of the keyboard. This allows you to set the trace specifications for state measurements.

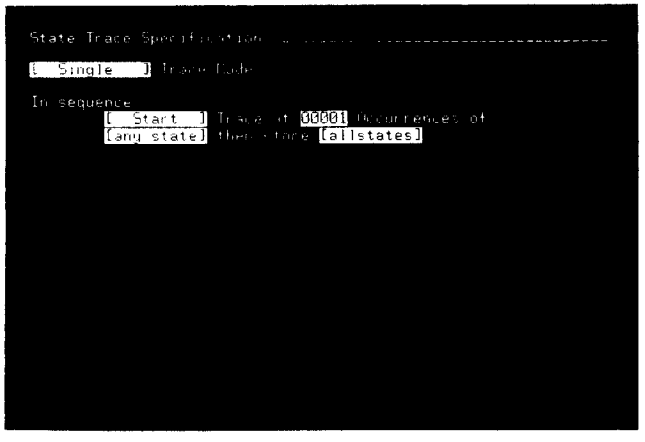


Figure 61

The first field in the menu, [Single], allows you to select the trace mode, whether single or continuous. Continuous is a series of single acquisitions. Each time the analyzer meets the specified trace condition, (trace=trigger+delay), it captures the data and goes on to another acquisition. In single mode, the first time rhe analyzer sees data that meets its trace specification, it fills its internal memory and stops.

The [Single]/[Continuous] field also gives you the option of selecting [Compare] and [Overview] modes. Each of these are covered in detail in the operating and programming manual, and will not be discussed here.

The next field allows you to set the analyzer for [Start], [Center], or [End] trace mode. This field tells the analyzer how to store information in its internal memory. In start, the analyzer finds the selected tracepoint and begins to fill its memory with data until it is full. If the field is changed to center, the analyzer places the selected tracepoint in the center of its memory and stores data on either side (before and after). In end trace mode, the analyzer stops immediately upon finding its tracepoint. This means that the memory is tilled with data that occurred before the tracepoint.

The field to the right of the trace mode lets you select some delay for the tracepoint, after the trigger point. Remember, in **a** logic analyzer, trace = trigger + delay.

The next field is for setting the actual trace selection. At power on, this field is [any state]. Using the NEXT[ ]/PREV[ ] keys, you can cycle through the choices provided. If you choose something other than [any state] or [no state], four fields will appear at the bottom of the screen. These are labelled a, b, c, and d, to relate to those shown in the trace selection field. When the four fields appear at the bottom of the screen, they are followed by XXXX (don't care). An address can be entered from the keyboard to tell the analyzer what to look for.